

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *     Zvector E7 instruction tests for VRR-b encoded:
				5 *
				6 *     E780 VFEE    - Vector Find Element Equal
				7 *     E781 VFENE   - Vector Find Element Not Equal
				8 *     E782 VFAE    - Vector Find Any Element Equal
				9 *
				10 *           James Wekel February 2025
				11 *****
				13 *****
				14 *
				15 *           basic instruction tests
				16 *
				17 *****
				18 *     This program tests proper functioning of the z/arch E7 VRR-b
				19 *     Vector Find Element Equal, Vector Find Element Not Equal and
				20 *     Vector Find Any Element Equal instructions.
				21 *     Exceptions are not tested.
				22 *
				23 *     PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 *     obvious coding errors.  None of the tests are thorough.  They are
				25 *     NOT designed to test all aspects of any of the instructions.
				26 *
				27 *****
				28 *
				29 *     *Testcase zvector-e7-06-Find
				30 *     *
				31 *     *     Zvector E7 instruction tests for VRR-b encoded:
				32 *     *
				33 *     *     E780 VFEE    - Vector Find Element Equal
				34 *     *     E781 VFENE   - Vector Find Element Not Equal
				35 *     *     E782 VFAE    - Vector Find Any Element Equal
				36 *     *
				37 *     *     # -----
				38 *     *     #     This tests only the basic function of the instruction.
				39 *     *     #     Exceptions are NOT tested.
				40 *     *     # -----
				41 *     *
				42 *     mainsize     2
				43 *     numcpu       1
				44 *     sysclear
				45 *     archlvl      z/Arch
				46 *
				47 *     loadcore     "\$ (testpath) /zvector-e7-06-Find.core" 0x0
				48 *
				49 *     diag8cmd     enable     # (needed for messages to Hercules console)
				50 *     runtest      10         #
				51 *     diag8cmd     disable    # (reset back to default)
				52 *
				53 *     *Done
				54 *
				55 *
				56 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				58 *****
				59 * FCHECK Macro - Is a Facility Bit set?
				60 *
				61 * If the facility bit is NOT set, an message is issued and
				62 * the test is skipped.
				63 *
				64 * Fcheck uses R0, R1 and R2
				65 *
				66 * eg. FCHECK 134, 'vector-packed-decimal'
				67 *****
				68 MACRO
				69 FCHECK &BITNO, &NOTSETMSG
				70 . * &BITNO : facility bit number to check
				71 . * &NOTSETMSG : 'facility name'
				72 LCLA &FBBYTE Facility bit in Byte
				73 LCLA &FBBIT Facility bit within Byte
				74
				75 LCLA &L(8)
				76 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				77
				78 &FBBYTE SETA &BITNO/8
				79 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				80 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				81
				82 B X&SYSNDX
				83 * Fcheck data area
				84 * skip messgae
				85 SKT&SYSNDX DC C' Skipping tests: '
				86 DC C&NOTSETMSG
				87 DC C' (bit &BITNO) is not installed.'
				88 SKL&SYSNDX EQU *-SKT&SYSNDX
				89 * facility bits
				90 DS FD gap
				91 FB&SYSNDX DS 4FD
				92 DS FD gap
				93 *
				94 X&SYSNDX EQU *
				95 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				96 STFLE FB&SYSNDX get facility bits
				97
				98 XGR R0, R0
				99 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				100 N R0, =F' &FBBIT' is bit set?
				101 BNZ XC&SYSNDX
				102 *
				103 * facility bit not set, issue message and exit
				104 *
				105 LA R0, SKL&SYSNDX message length
				106 LA R1, SKT&SYSNDX message address
				107 BAL R2, MSG
				108
				109 B EOJ
				110 XC&SYSNDX EQU *
				111 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				113	*****		
				114	* Low core PSWs		
				115	*****		
00000000		00000000	00004B33	116	ZVE7TST START 0		
		00000000		117	USING ZVE7TST, R0	Low core addressability	
				118			
		00000140	00000000	119	SVOLDPSW EQU ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
00000000		00000000	000001A0	121	ORG ZVE7TST+X' 1A0'	z/Architecture RESTART PSW	
000001A0	00000001 80000000			122	DC X' 0000000180000000'		
000001A8	00000000 00000200			123	DC AD(BEGIN)		
000001B0		000001B0	000001D0	125	ORG ZVE7TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW	
000001D0	00020001 80000000			126	DC X' 0002000180000000'		
000001D8	00000000 0000DEAD			127	DC AD(X' DEAD')		
000001E0		000001E0	00000200	129	ORG ZVE7TST+X' 200'	Start of actual test program..	
				131	*****		
				132	* The actual "ZVE7TST" program itself...		
				133	*****		
				134	* Architecture Mode: z/Arch		
				135	* Register Usage:		
				136	* R0 (work)		
				137	* R1-4 (work)		
				138	* R5 Testing control table - current test base		
				139	* R6- R7 (work)		
				140	* R8 First base register		
				141	* R9 Second base register		
				142	* R10 Third base register		
				143	* R11 E7TEST call return		
				144	* R12 E7TESTS register		
				145	* R13 (work)		
				146	* R14 Subroutine call		
				147	* R15 Secondary Subroutine call or work		
				148	* R15 Secondary Subroutine call or work		
				149	* R15 Secondary Subroutine call or work		
				150	* R15 Secondary Subroutine call or work		
				151	*****		
00000200		00000200		153	USING BEGIN, R8	FIRST Base Register	
00000200		00001200		154	USING BEGIN+4096, R9	SECOND Base Register	
00000200		00002200		155	USING BEGIN+8192, R10	THIRD Base Register	
00000200	0580			157	BEGIN BALR R8, 0	Inititalize FIRST base register	
00000202	0680			158	BCTR R8, 0	Inititalize FIRST base register	
00000204	0680			159	BCTR R8, 0	Inititalize FIRST base register	
00000206	4190 8800		00000800	161	LA R9, 2048(, R8)	Inititalize SECOND base register	
0000020A	4190 9800		00000800	162	LA R9, 2048(, R9)	Inititalize SECOND base register	
				163			





LOC	OBJECT CODE			ADDR1	ADDR2	STMT	
						239	*****
						240	* cc was not as expected
				0000031C	00000001	241	*****
						242	CCMSG EQU *
						243	*
						244	* is CS set by test?
						245	*
0000031C	E310	5008	0076		00000008	246	LB R1, M5 Get M5
00000322	E310	8360	0080		00000560	247	NG R1, =D' 1' isolate CS
00000328	4780	8100			00000300	248	BZ TESTREST not set?
						249	*
						250	* extract CC from extracted PSW
						251	*
0000032C	5810	500C			0000000C	252	L R1, CCPSW
00000330	8810	000C			0000000C	253	SRL R1, 12
00000334	5410	8370			00000570	254	N R1, =XL4' 3'
00000338	4210	5014			00000014	255	STC R1, CCFOUND save cc
						256	*
						257	* FILL IN MESSAGE
						258	*
0000033C	4820	5004			00000004	259	LH R2, TNUM get test number and convert
00000340	4E20	8ED6			000010D6	260	CVD R2, DECNUM
00000344	D211	8EC0	8EAA	000010C0	000010AA	261	MVC PRT3, EDIT
0000034A	DE11	8EC0	8ED6	000010C0	000010D6	262	ED PRT3, DECNUM
00000350	D202	8E65	8ECD	00001065	000010CD	263	MVC CCPRTNUM(3), PRT3+13 fill in message with test #
						264	
00000356	D207	8E82	5015	00001082	00000015	265	MVC CCPRTNAME, OPNAME fill in message with instruction
						266	
0000035C	B982	0022				267	XGR R2, R2 get CC as U8
00000360	4320	5009			00000009	268	IC R2, CC
00000364	4E20	8ED6			000010D6	269	CVD R2, DECNUM and convert
00000368	D211	8EC0	8EAA	000010C0	000010AA	270	MVC PRT3, EDIT
0000036E	DE11	8EC0	8ED6	000010C0	000010D6	271	ED PRT3, DECNUM
00000374	D200	8E98	8ECF	00001098	000010CF	272	MVC CCPRTEXP(1), PRT3+15 fill in message with CC field
						273	
0000037A	B982	0022				274	XGR R2, R2 get CCFOUND as U8
0000037E	4320	5014			00000014	275	IC R2, CCFOUND
00000382	4E20	8ED6			000010D6	276	CVD R2, DECNUM and convert
00000386	D211	8EC0	8EAA	000010C0	000010AA	277	MVC PRT3, EDIT
0000038C	DE11	8EC0	8ED6	000010C0	000010D6	278	ED PRT3, DECNUM
00000392	D200	8EA8	8ECF	000010A8	000010CF	279	MVC CCPRTGOT(1), PRT3+15 fill in message with ccfound
						280	
00000398	4100	0055			00000055	281	LA R0, CCPRTLNG message length
0000039C	4110	8E55			00001055	282	LA R1, CCPRTLNE messagfe address
000003A0	45F0	8236			00000436	283	BAL R15, RPTERROR
						284	
000003A4	5800	8374			00000574	285	L R0, =F' 1' set failed test indicator
000003A8	5000	8E00			00001000	286	ST R0, FAILED
						287	
000003AC	47F0	8100			00000300	288	B TESTREST
						289	



LOC	OBJECT CODE			ADDR1	ADDR2	STMT	
						291 *****	
						292 * result not as expected:	
						293 * issue message with test number, instruction under test	
						294 * and instruction m4, m5	
						295 *****	
				000003B0	00000001	296 FAILMSG EQU *	
000003B0	4820	5004			00000004	297 LH R2, TNUM	get test number and convert
000003B4	4E20	8ED6			000010D6	298 CVD R2, DECNUM	
000003B8	D211	8EC0 8EAA		000010C0	000010AA	299 MWC PRT3, EDIT	
000003BE	DE11	8EC0 8ED6		000010C0	000010D6	300 ED PRT3, DECNUM	
000003C4	D202	8E18 8ECD		00001018	000010CD	301 MWC PRTNUM(3), PRT3+13	fill in message with test #
						302	
000003CA	D207	8E33 5015		00001033	00000015	303 MWC PRTNAME, OPNAME	fill in message with instruction
						304	
000003D0	B982	0022				305 XGR R2, R2	get M4 as U8
000003D4	4320	5007			00000007	306 IC R2, M4	
000003D8	4E20	8ED6			000010D6	307 CVD R2, DECNUM	and convert
000003DC	D211	8EC0 8EAA		000010C0	000010AA	308 MWC PRT3, EDIT	
000003E2	DE11	8EC0 8ED6		000010C0	000010D6	309 ED PRT3, DECNUM	
000003E8	D202	8E44 8ECD		00001044	000010CD	310 MWC PRTM4(3), PRT3+13	fill in message with M4 field
						311	
000003EE	B982	0022				312 XGR R2, R2	get M5 as U8
000003F2	4320	5008			00000008	313 IC R2, M5	
000003F6	4E20	8ED6			000010D6	314 CVD R2, DECNUM	and convert
000003FA	D211	8EC0 8EAA		000010C0	000010AA	315 MWC PRT3, EDIT	
00000400	DE11	8EC0 8ED6		000010C0	000010D6	316 ED PRT3, DECNUM	
00000406	D202	8E51 8ECD		00001051	000010CD	317 MWC PRTM5(3), PRT3+13	fill in message with M5 field
						318	
0000040C	4100	004D			0000004D	319 LA R0, PRTLNG	message length
00000410	4110	8E08			00001008	320 LA R1, PRTLNE	messagfe address
00000414	45F0	8236			00000436	321 BAL R15, RPTERROR	
						323 *****	
						324 * continue after a failed test	
						325 *****	
				00000418	00000001	326 FAILCONT EQU *	
00000418	5800	8374			00000574	327 L R0, =F' 1'	set failed test indicator
0000041C	5000	8E00			00001000	328 ST R0, FAILED	
						329	
00000420	41C0	C004			00000004	330 LA R12, 4(0, R12)	next test address
00000424	47F0	80D4			000002D4	331 B NEXTE7	
						333 *****	
						334 * end of testing; set ending psw	
						335 *****	
				00000428	00000001	336 ENDTEST EQU *	
00000428	5810	8E00			00001000	337 L R1, FAILED	did a test fail?
0000042C	1211					338 LTR R1, R1	
0000042E	4780	8338			00000538	339 BZ EOJ	No, exit
00000432	47F0	8350			00000550	340 B FAILTEST	Yes, exit with BAD PSW

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				342	*****			
				343	*	RPTERROR	Report instruction test in error	
				344	*		R0 = MESSGAE LENGTH	
				345	*		R1 = ADDRESS OF MESSAGE	
				346	*****			
00000436	50F0 8254		00000454	348	RPTERROR	ST	R15, RPTSAVE	Save return address
0000043A	5050 8258		00000458	349		ST	R5, RPTSVR5	Save R5
				350	*			
				351	*	Use Hercules Diagnose for Message to console		
				352	*			
0000043E	9002 8260		00000460	353		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000442	4520 8270		00000470	354		BAL	R2, MSG	call Hercules console MSG display
00000446	9802 8260		00000460	355		LM	R0, R2, RPTDWSAV	restore regs
0000044A	5850 8258		00000458	357		L	R5, RPTSVR5	Restore R5
0000044E	58F0 8254		00000454	358		L	R15, RPTSAVE	Restore return address
00000452	07FF			359		BR	R15	Return to caller
00000454	00000000			361	RPTSAVE	DC	F' 0'	R15 save area
00000458	00000000			362	RPTSVR5	DC	F' 0'	R5 save area
00000460	00000000 00000000			364	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call
				366	*****			
				367	*	Issue HERCULES MESSAGE pointed to by R1, length in R0		
				368	*	R2 = return address		
				369	*****			
00000470	4900 8378		00000578	371	MSG	CH	R0, =H' 0'	Do we even HAVE a message?
00000474	07D2			372		BNHR	R2	No, ignore
00000476	9002 82AC		000004AC	374		STM	R0, R2, MSGSAVE	Save registers
0000047A	4900 837A		0000057A	376		CH	R0, =AL2(L' MSGMSG)	Message length within limits?
0000047E	47D0 8286		00000486	377		BNH	MSGOK	Yes, continue
00000482	4100 005F		0000005F	378		LA	R0, L' MSGMSG	No, set to maximum
00000486	1820			380	MSGOK	LR	R2, R0	Copy length to work register
00000488	0620			381		BCTR	R2, 0	Minus-1 for execute
0000048A	4420 82B8		000004B8	382		EX	R2, MSGMVC	Copy message to O/P buffer
0000048E	4120 200A		0000000A	384		LA	R2, 1+L' MSGCMD(, R2)	Calculate true command length
00000492	4110 82BE		000004BE	385		LA	R1, MSGCMD	Point to true command
00000496	83120008			387		DC	X' 83' , X' 12' , X' 0008'	Issue Hercules Diagnose X' 008'
0000049A	4780 82A6		000004A6	388		BZ	MSGRET	Return if successful
				389				
0000049E	1222			390		LTR	R2, R2	Is Diag8 Ry (R2) 0?
000004A0	4780 82A6		000004A6	391		BZ	MSGRET	an error occurred but coninue
				392				
000004A4	0000			393		DC	H' 0'	CRASH for debugging purposes
000004A6	9802 82AC		000004AC	395	MSGRET	LM	R0, R2, MSGSAVE	Restore registers







LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				443 *=====
				444 *
				445 * NOTE: start data on an address that is easy to display
				446 * within Hercules
				447 *
				448 *=====
				449
0000057C		0000057C	00001000	450 ORG ZVE7TST+X' 1000'
00001000	00000000			451 FAILED DC F' 0' some test failed?
00001004	00000000			452 TESTING DC F' 0' current test number
				454 *****
				455 * TEST failed : result messgae
				456 *****
				457 *
				458 * failed message and associated editing
				459 *
00001008	40404040	40404040		460 PRTLNE DC C' Test # '
00001018	A7A7A7			461 PRTNUM DC C' xxx'
0000101B	40868189	93858440		462 DC C' failed for instruction '
00001033	A7A7A7A7	A7A7A7A7		463 PRTNAME DC CL8' xxxxxxxx'
0000103B	40A689A3	884094F4		464 DC C' with m4=
00001044	A7A7A7			465 PRTM4 DC C' xxx'
00001047	6B			466 DC C' ,'
00001048	40A689A3	884094F5		467 DC C' with m5=
00001051	A7A7A7			468 PRTM5 DC C' xxx'
00001054	4B			469 DC C' .'
		0000004D	00000001	470 PRTLNG EQU *- PRTLNE
				471
				472 *****
				473 * TEST failed : CC message
				474 *****
				475 *
				476 * failed message and associated editing
				477 *
00001055	40404040	40404040		478 CCPRTLNE DC C' Test # '
00001065	A7A7A7			479 CCPRTNUM DC C' xxx'
00001068	40A69996	95874083		480 DC c' wrong cc for instruction '
00001082	A7A7A7A7	A7A7A7A7		481 CCPRTNAME DC CL8' xxxxxxxx'
0000108A	4085A797	8583A385		482 DC C' expected: cc=
00001098	A7			483 CCPRTEXP DC C' x'
00001099	6B			484 DC C' ,'
0000109A	40998583	8589A585		485 DC C' received: cc=
000010A8	A7			486 CCPRTGOT DC C' x'
000010A9	4B			487 DC C' .'
		00000055	00000001	488 CCPRTLNG EQU *- CCPRTLNE

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				490 *****
				491 * TEST failed : message working storge
				492 *****
000010AA	40212020	20202020		493 EDIT DC XL18' 40212020202020202020202020202020'
				494
000010BC	7E7E7E6E			495 DC C' ==>'
000010C0	40404040	40404040		496 PRT3 DC CL18' '
000010D2	4C7E7E7E			497 DC C' <==='
000010D6	00000000	00000000		498 DECNUM DS CL16
				500 *****
				501 * Vector instruction results, pollution and input
				502 *****
000010E8				503 DS 0F
000010E8	00000000	00000000		504 DS XL16
000010F8	FFFFFFFF	FFFFFFFF		505 V1FUDGE DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF' gap
00001108	00000000	00000000		506 DS XL16 V1 FUDGE
				508 *****
				509 * E7TEST DSECT
				510 *****
				512 E7TEST DSECT ,
00000000	00000000			513 TSUB DC A(0) pointer to test
00000004	0000			514 TNUM DC H' 00' Test Number
00000006	00			515 DC X' 00'
00000007	00			516 M4 DC HL1' 00' m4 used
00000008	00			517 M5 DC HL1' 00' m5 used
00000009	00			518 CC DC HL1' 00' cc expected
0000000A	00			519 CCMASK DC HL1' 00' not expected CC mask
				520 *
				521 * CC extrtaction
				522 *
0000000C	00000000	00000000		523 CCPSW DS 2F extract PSW after test (has CC)
00000014	00			524 CCFOUND DS X extracted cc
				525
00000015	40404040	40404040		526 OPNAME DC CL8' ' E7 name
00000020	00000000			527 V1ADDR DC A(0) address of v1 result
00000024	00000000			528 V2ADDR DC A(0) address of v2 source
00000028	00000000			529 V3ADDR DC A(0) address of v3 source
0000002C	00000000			530 RELEN DC A(0) RESULT LENGTH
00000030	00000000			531 READDR DC A(0) result (expected) address
00000038	00000000	00000000		532 DS FD gap
00000040	00000000	00000000		533 V1OUTPUT DS XL16 V1 Output
00000050	00000000	00000000		534 DS FD gap
				535
				536 * test routine will be here (from VRR- b macro)
				537 *
				538 * followed by
				539 * EXPECTED RESULT

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
00001118		00000000	00004B33	541 ZVE7TST CSECT , 542 DS OF	
				544 *****	
				545 * Macros to help build test tables	
				546 *****	
				548 *	
				549 * macro to generate individual test	
				550 *	
				551 MACRO	
				552 VRR_B &INST, &M4, &M5, &CC	
				553 . *	&INST - VRR-b instruction under test
				554 . *	&M4 - m4 field - element size
				555 . *	&M5 - m5 field - IN, RT, ZS, CS
				556 . *	&CC - expected CC
				557	
				558 LCLA &XCC(4) &XCC has mask values for FAILED condition codes	
				559 &XCC(1) SETA 7	CC != 0
				560 &XCC(2) SETA 11	CC != 1
				561 &XCC(3) SETA 13	CC != 2
				562 &XCC(4) SETA 14	CC != 3
				563	
				564 GBLA &TNUM	
				565 &TNUM SETA &TNUM+1	
				566	
				567 DS OFD	
				568 USING *, R5	base for test data and test routine
				569	
				570 T&TNUM DC A(X&TNUM)	address of test routine
				571 DC H' &TNUM	test number
				572 DC X' 00'	
				573 DC HL1' &M4'	m4 used
				574 DC HL1' &M5'	m5 used
				575 DC HL1' &CC'	CC
				576 DC HL1' &XCC(&CC+1)'	CC failed mask
				577	
				578 DS 2F	extracted PSW after test (has CC)
				579 DC X' FF'	extracted CC, if test failed
				580	
				581 DC CL8' &INST'	instruction name
				582 DC A(RE&TNUM)	address of v1 result
				583 DC A(RE&TNUM+16)	address of v2 source
				584 DC A(RE&TNUM+32)	address of v3 source
				585 DC A(16)	result length
				586 REA&TNUM DC A(RE&TNUM)	result address
				587 DS FD	gap
				588 V10&TNUM DS XL16	V1 output
				589 DS FD	gap
				590 . *	
				591 *	
				592 X&TNUM DS OF	
				593 LGF R1, V2ADDR	load v2 source
				594 VL v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				595	LGF R1, V3ADDR
				596	VL v23, 0(R1)
				597	
				598	&INST V21, V22, V23, &M4, &M5
				599	test instruction
				600	EPSW R2, R0
				601	ST R2, CCPSW
				602	
				603	VST V21, V10&TNUM
				604	save v1 output
				605	BR R11
				606	return
				607	RE&TNUM DC 0F
				608	V1 for this test
				609	DROP R5
				610	MEND
				612	*
				613	* macro to generate table of pointers to individual tests
				614	*
				615	MACRO
				616	PTTABLE
				617	GBLA &TNUM
				618	LCLA &CUR
				619	&CUR SETA 1
				620	. *
				621	TTABLE DS 0F
				622	. LOOP
				623	. *
				624	DC A(T&CUR)
				625	. *
				626	&CUR SETA &CUR+1
				627	AIF (&CUR LE &TNUM) . LOOP
				628	*
				629	DC A(0)
				630	DC A(0)
				631	. *
				632	MEND
				633	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				635 *****
				636 * E7 VRR-b tests
				637 *****
				638 PRINT DATA
				639 *
				640 *
				641 * E780 VFEE - Vector Find Element Equal
				642 * E781 VFENE - Vector Find Element Not Equal
				643 * E782 VFAE - Vector Find Any Element Equal
				644 *
				645 * VRR-b instruction,
				646 * M4, element size
				647 * M5, IN, RT, ZS, CS
				648 * CC expected condition code
				649 *
				650 * followed by
				651 * 16 byte V1 result
				652 * 16 byte V2 source
				653 * 16 byte V3 source
				654 *
				655 * -----
				656 * VFEE - Vector Find Element Equal
				657 * -----
				658
				659 * -----
				660 * case 0 - simple debug CC=1 ZS=0, CS=1
				661 * -----
				662 *
				663 VRR_B VFEE, 0, 1, 1
00001118				664+ DS OFD
00001118		00001118		665+ USING *, R5 base for test data and test routine
00001118	00001170			666+T1 DC A(X1) address of test routine
0000111C	0001			667+ DC H' 1' test number
0000111E	00			668+ DC X' 00'
0000111F	00			669+ DC HL1' 0' m4 used
00001120	01			670+ DC HL1' 1' m5 used
00001121	01			671+ DC HL1' 1' CC
00001122	0B			672+ DC HL1' 11' CC failed mask
00001124	00000000 00000000			673+ DS 2F extracted PSW after test (has CC)
0000112C	FF			674+ DC X' FF' extracted CC, if test failed
0000112D	E5C6C5C5 40404040			675+ DC CL8' VFEE' instruction name
00001138	000011A0			676+ DC A(RE1) address of v1 result
0000113C	000011B0			677+ DC A(RE1+16) address of v2 source
00001140	000011C0			678+ DC A(RE1+32) address of v3 source
00001144	00000010			679+ DC A(16) result length
00001148	000011A0			680+REA1 DC A(RE1) result address
00001150	00000000 00000000			681+ DS FD gap
00001158	00000000 00000000			682+V101 DS XL16 V1 output
00001160	00000000 00000000			
00001168	00000000 00000000			683+ DS FD gap
				684+*
00001170				685+X1 DS OF
00001170	E310 5024 0014	00000024		686+ LGF R1, V2ADDR load v2 source
00001176	E761 0000 0806	00000000		687+ VL v22, 0(R1) use v21 to test decoder
0000117C	E310 5028 0014	00000028		688+ LGF R1, V3ADDR load v3 source
00001182	E771 0000 0806	00000000		689+ VL v23, 0(R1) use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001188	E756 7010 0E80			690+	VFEE	V21, V22, V23, 0, 1	test instruction
0000118E	B98D 0020			691+	EPSW	R2, R0	extract psw
00001192	5020 500C		0000000C	692+	ST	R2, CCPSW	to save CC
00001196	E750 5040 080E		00001158	693+	VST	V21, V101	save v1 output
0000119C	07FB			694+	BR	R11	return
000011A0				695+RE1	DC	0F	V1 for this test
000011A0				696+	DROP	R5	
000011A0	00000000 00000000			697	DC	XL16' 00000000000000000000000000000000'	V1
000011A8	00000000 00000000						
000011B0	00000000 00000000			698	DC	XL16' 00000000000000000000000000000000'	v2
000011B8	00000000 00000000						
000011C0	00000000 00000000			699	DC	XL16' 00000000000000000000000000000000'	v3
000011C8	00000000 00000000						
				700			
				701	*	-----	
				702	*	case 1 - Hardware Verified	
				703	*	-----	
				704	*	Byte, No equal, no zero	cc=3
				705	VRR_B	VFEE, 0, 3, 3	
000011D0				706+	DS	0FD	
000011D0		000011D0		707+	USING	*, R5	base for test data and test routine
000011D0	00001228			708+T2	DC	A(X2)	address of test routine
000011D4	0002			709+	DC	H' 2'	test number
000011D6	00			710+	DC	X' 00'	
000011D7	00			711+	DC	HL1' 0'	m4 used
000011D8	03			712+	DC	HL1' 3'	m5 used
000011D9	03			713+	DC	HL1' 3'	CC
000011DA	0E			714+	DC	HL1' 14'	CC failed mask
000011DC	00000000 00000000			715+	DS	2F	extracted PSW after test (has CC)
000011E4	FF			716+	DC	X' FF'	extracted CC, if test failed
000011E5	E5C6C5C5 40404040			717+	DC	CL8' VFEE'	instruction name
000011F0	00001258			718+	DC	A(RE2)	address of v1 result
000011F4	00001268			719+	DC	A(RE2+16)	address of v2 source
000011F8	00001278			720+	DC	A(RE2+32)	address of v3 source
000011FC	00000010			721+	DC	A(16)	result length
00001200	00001258			722+REA2	DC	A(RE2)	result address
00001208	00000000 00000000			723+	DS	FD	gap
00001210	00000000 00000000			724+V102	DS	XL16	V1 output
00001218	00000000 00000000						
00001220	00000000 00000000			725+	DS	FD	gap
				726+*			
00001228				727+X2	DS	0F	
00001228	E310 5024 0014		00000024	728+	LGF	R1, V2ADDR	load v2 source
0000122E	E761 0000 0806		00000000	729+	VL	v22, 0(R1)	use v21 to test decoder
00001234	E310 5028 0014		00000028	730+	LGF	R1, V3ADDR	load v3 source
0000123A	E771 0000 0806		00000000	731+	VL	v23, 0(R1)	use v22 to test decoder
00001240	E756 7030 0E80			732+	VFEE	V21, V22, V23, 0, 3	test instruction
00001246	B98D 0020			733+	EPSW	R2, R0	extract psw
0000124A	5020 500C		0000000C	734+	ST	R2, CCPSW	to save CC
0000124E	E750 9010 080E		00001210	735+	VST	V21, V102	save v1 output
00001254	07FB			736+	BR	R11	return
00001258				737+RE2	DC	0F	V1 for this test
00001258				738+	DROP	R5	
00001258	00000000 00000010			739	DC	XL16' 00000000000000001000000000000000'	V1
00001260	00000000 00000000						
00001268	5D3A5859 5A535953			740	DC	XL16' 5D3A58595A53595354454D445F444546'	v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001270	54454D44 5F444546						
00001278	25252525 25252525			741	DC	XL16' 25252525252525252525252525252525'	v3
00001280	25252525 25252525						
				742			
				743	* Byte, No equal, with zero	cc=0	
				744	VRR_B VFEE, 0, 3, 0		
00001288				745+	DS	OFD	
00001288		00001288		746+	USING	*, R5	base for test data and test routine
00001288	000012E0			747+T3	DC	A(X3)	address of test routine
0000128C	0003			748+	DC	H' 3'	test number
0000128E	00			749+	DC	X' 00'	
0000128F	00			750+	DC	HL1' 0'	m4 used
00001290	03			751+	DC	HL1' 3'	m5 used
00001291	00			752+	DC	HL1' 0'	CC
00001292	07			753+	DC	HL1' 7'	CC failed mask
00001294	00000000 00000000			754+	DS	2F	extracted PSW after test (has CC)
0000129C	FF			755+	DC	X' FF'	extracted CC, if test failed
0000129D	E5C6C5C5 40404040			756+	DC	CL8' VFEE'	instruction name
000012A8	00001310			757+	DC	A(RE3)	address of v1 result
000012AC	00001320			758+	DC	A(RE3+16)	address of v2 source
000012B0	00001330			759+	DC	A(RE3+32)	address of v3 source
000012B4	00000010			760+	DC	A(16)	result length
000012B8	00001310			761+REA3	DC	A(RE3)	result address
000012C0	00000000 00000000			762+	DS	FD	gap
000012C8	00000000 00000000			763+V103	DS	XL16	V1 output
000012D0	00000000 00000000						
000012D8	00000000 00000000			764+	DS	FD	gap
				765+*			
000012E0				766+X3	DS	0F	
000012E0	E310 5024 0014		00000024	767+	LGF	R1, V2ADDR	load v2 source
000012E6	E761 0000 0806		00000000	768+	VL	v22, 0(R1)	use v21 to test decoder
000012EC	E310 5028 0014		00000028	769+	LGF	R1, V3ADDR	load v3 source
000012F2	E771 0000 0806		00000000	770+	VL	v23, 0(R1)	use v22 to test decoder
000012F8	E756 7030 0E80			771+	VFEE	V21, V22, V23, 0, 3	test instruction
000012FE	B98D 0020			772+	EPSW	R2, R0	extract psw
00001302	5020 500C		0000000C	773+	ST	R2, CCPSW	to save CC
00001306	E750 5040 080E		000012C8	774+	VST	V21, V103	save v1 output
0000130C	07FB			775+	BR	R11	return
00001310				776+RE3	DC	0F	V1 for this test
00001310				777+	DROP	R5	
00001310	00000000 00000009			778	DC	XL16' 00000000000000009000000000000000'	V1
00001318	00000000 00000000						
00001320	5D3A5859 5A535953			779	DC	XL16' 5D3A58595A53595354004D445F444546'	v2
00001328	54004D44 5F444546						
00001330	25252525 25252525			780	DC	XL16' 25252525252525252525002525252525'	v3
00001338	25002525 25252525						
				781			
				782	* Byte, Equal, no zero	cc=1	
				783	VRR_B VFEE, 0, 3, 1		
00001340				784+	DS	OFD	
00001340		00001340		785+	USING	*, R5	base for test data and test routine
00001340	00001398			786+T4	DC	A(X4)	address of test routine
00001344	0004			787+	DC	H' 4'	test number
00001346	00			788+	DC	X' 00'	
00001347	00			789+	DC	HL1' 0'	m4 used
00001348	03			790+	DC	HL1' 3'	m5 used

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001349	01			791+	DC	HL1' 1'
0000134A	0B			792+	DC	HL1' 11'
0000134C	00000000 00000000			793+	DS	2F
00001354	FF			794+	DC	X' FF'
00001355	E5C6C5C5 40404040			795+	DC	CL8' VFEE'
00001360	000013C8			796+	DC	A(RE4)
00001364	000013D8			797+	DC	A(RE4+16)
00001368	000013E8			798+	DC	A(RE4+32)
0000136C	00000010			799+	DC	A(16)
00001370	000013C8			800+REA4	DC	A(RE4)
00001378	00000000 00000000			801+	DS	FD
00001380	00000000 00000000			802+V104	DS	XL16
00001388	00000000 00000000					
00001390	00000000 00000000			803+	DS	FD
				804+*		gap
00001398				805+X4	DS	0F
00001398	E310 5024 0014		00000024	806+	LGF	R1, V2ADDR
0000139E	E761 0000 0806		00000000	807+	VL	v22, 0(R1)
000013A4	E310 5028 0014		00000028	808+	LGF	R1, V3ADDR
000013AA	E771 0000 0806		00000000	809+	VL	v23, 0(R1)
000013B0	E756 7030 0E80			810+	VFEE	V21, V22, V23, 0, 3
000013B6	B98D 0020			811+	EPSW	R2, R0
000013BA	5020 500C		0000000C	812+	ST	R2, CCPSW
000013BE	E750 5040 080E		00001380	813+	VST	V21, V104
000013C4	07FB			814+	BR	R11
000013C8				815+RE4	DC	0F
000013C8				816+	DROP	R5
000013C8	00000000 00000005			817	DC	XL16' 00000000000000005000000000000000' V1
000013D0	00000000 00000000					
000013D8	5D3A5859 5A255953			818	DC	XL16' 5D3A58595A25595354454D445F444546' v2
000013E0	54454D44 5F444546					
000013E8	25252525 25252525			819	DC	XL16' 25252525252525252525252525252525' v3
000013F0	25252525 25252525					
				820		
				821 * Byte, Equal before zero		cc=2
				822	VRR_B	VFEE, 0, 3, 2
000013F8				823+	DS	0FD
000013F8		000013F8		824+	USING	*, R5
000013F8	00001450			825+T5	DC	A(X5)
000013FC	0005			826+	DC	H' 5'
000013FE	00			827+	DC	X' 00'
000013FF	00			828+	DC	HL1' 0'
00001400	03			829+	DC	HL1' 3'
00001401	02			830+	DC	HL1' 2'
00001402	0D			831+	DC	HL1' 13'
00001404	00000000 00000000			832+	DS	2F
0000140C	FF			833+	DC	X' FF'
0000140D	E5C6C5C5 40404040			834+	DC	CL8' VFEE'
00001418	00001480			835+	DC	A(RE5)
0000141C	00001490			836+	DC	A(RE5+16)
00001420	000014A0			837+	DC	A(RE5+32)
00001424	00000010			838+	DC	A(16)
00001428	00001480			839+REA5	DC	A(RE5)
00001430	00000000 00000000			840+	DS	FD
00001438	00000000 00000000			841+V105	DS	XL16
00001440	00000000 00000000					V1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001448	00000000 00000000			842+ 843+*	DS	FD	gap
00001450				844+X5	DS	OF	
00001450	E310 5024 0014		00000024	845+	LGF	R1, V2ADDR	load v2 source
00001456	E761 0000 0806		00000000	846+	VL	v22, 0(R1)	use v21 to test decoder
0000145C	E310 5028 0014		00000028	847+	LGF	R1, V3ADDR	load v3 source
00001462	E771 0000 0806		00000000	848+	VL	v23, 0(R1)	use v22 to test decoder
00001468	E756 7030 0E80			849+	VFEE	V21, V22, V23, 0, 3	test instruction
0000146E	B98D 0020			850+	EPSW	R2, R0	extract psw
00001472	5020 500C		0000000C	851+	ST	R2, CCPSW	to save CC
00001476	E750 5040 080E		00001438	852+	VST	V21, V105	save v1 output
0000147C	07FB			853+	BR	R11	return
00001480				854+RE5	DC	OF	V1 for this test
00001480				855+	DROP	R5	
00001480	00000000 00000005			856	DC	XL16' 00000000000000005000000000000000'	V1
00001488	00000000 00000000						
00001490	5D3A5859 5A255953			857	DC	XL16' 5D3A58595A25595354004D445F444546'	v2
00001498	54004D44 5F444546						
000014A0	25252525 25252525			858	DC	XL16' 25252525252525252525252525252525'	v3
000014A8	25252525 25252525						
				859			
				860 * Byte, Equal after zero			cc=0
				861	VRR_B	VFEE, 0, 3, 0	
000014B0				862+	DS	OFD	
000014B0		000014B0		863+	USING	*, R5	base for test data and test routine
000014B0	00001508			864+T6	DC	A(X6)	address of test routine
000014B4	0006			865+	DC	H' 6'	test number
000014B6	00			866+	DC	X' 00'	
000014B7	00			867+	DC	HL1' 0'	m4 used
000014B8	03			868+	DC	HL1' 3'	m5 used
000014B9	00			869+	DC	HL1' 0'	CC
000014BA	07			870+	DC	HL1' 7'	CC failed mask
000014BC	00000000 00000000			871+	DS	2F	extracted PSW after test (has CC)
000014C4	FF			872+	DC	X' FF'	extracted CC, if test failed
000014C5	E5C6C5C5 40404040			873+	DC	CL8' VFEE'	instruction name
000014D0	00001538			874+	DC	A(RE6)	address of v1 result
000014D4	00001548			875+	DC	A(RE6+16)	address of v2 source
000014D8	00001558			876+	DC	A(RE6+32)	address of v3 source
000014DC	00000010			877+	DC	A(16)	result length
000014E0	00001538			878+REA6	DC	A(RE6)	result address
000014E8	00000000 00000000			879+	DS	FD	gap
000014F0	00000000 00000000			880+V106	DS	XL16	V1 output
000014F8	00000000 00000000						
00001500	00000000 00000000			881+	DS	FD	gap
				882+*			
00001508				883+X6	DS	OF	
00001508	E310 5024 0014		00000024	884+	LGF	R1, V2ADDR	load v2 source
0000150E	E761 0000 0806		00000000	885+	VL	v22, 0(R1)	use v21 to test decoder
00001514	E310 5028 0014		00000028	886+	LGF	R1, V3ADDR	load v3 source
0000151A	E771 0000 0806		00000000	887+	VL	v23, 0(R1)	use v22 to test decoder
00001520	E756 7030 0E80			888+	VFEE	V21, V22, V23, 0, 3	test instruction
00001526	B98D 0020			889+	EPSW	R2, R0	extract psw
0000152A	5020 500C		0000000C	890+	ST	R2, CCPSW	to save CC
0000152E	E750 5040 080E		000014F0	891+	VST	V21, V106	save v1 output
00001534	07FB			892+	BR	R11	return
00001538				893+RE6	DC	OF	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001538				894+	DROP	R5	
00001538	00000000 00000005			895	DC	XL16' 00000000000000050000000000000000'	V1
00001540	00000000 00000000						
00001548	5D3A5859 5A005953			896	DC	XL16' 5D3A58595A00595354254D445F444546'	v2
00001550	54254D44 5F444546						
00001558	25252525 25252525			897	DC	XL16' 25252525252525252525252525252525'	v3
00001560	25252525 25252525						
				898			
				899	* Halfword, No equal, no zero		cc=3
				900	VRR_B	VFEE, 1, 3, 3	
00001568				901+	DS	0FD	
00001568		00001568		902+	USING	*, R5	base for test data and test routine
00001568	000015C0			903+T7	DC	A(X7)	address of test routine
0000156C	0007			904+	DC	H' 7'	test number
0000156E	00			905+	DC	X' 00'	
0000156F	01			906+	DC	HL1' 1'	m4 used
00001570	03			907+	DC	HL1' 3'	m5 used
00001571	03			908+	DC	HL1' 3'	CC
00001572	0E			909+	DC	HL1' 14'	CC failed mask
00001574	00000000 00000000			910+	DS	2F	extracted PSW after test (has CC)
0000157C	FF			911+	DC	X' FF'	extracted CC, if test failed
0000157D	E5C6C5C5 40404040			912+	DC	CL8' VFEE'	instruction name
00001588	000015F0			913+	DC	A(RE7)	address of v1 result
0000158C	00001600			914+	DC	A(RE7+16)	address of v2 source
00001590	00001610			915+	DC	A(RE7+32)	address of v3 source
00001594	00000010			916+	DC	A(16)	result length
00001598	000015F0			917+REA7	DC	A(RE7)	result address
000015A0	00000000 00000000			918+	DS	FD	gap
000015A8	00000000 00000000			919+V107	DS	XL16	V1 output
000015B0	00000000 00000000						
000015B8	00000000 00000000			920+	DS	FD	gap
				921+*			
000015C0				922+X7	DS	0F	
000015C0	E310 5024 0014		00000024	923+	LGF	R1, V2ADDR	load v2 source
000015C6	E761 0000 0806		00000000	924+	VL	v22, 0(R1)	use v21 to test decoder
000015CC	E310 5028 0014		00000028	925+	LGF	R1, V3ADDR	load v3 source
000015D2	E771 0000 0806		00000000	926+	VL	v23, 0(R1)	use v22 to test decoder
000015D8	E756 7030 1E80			927+	VFEE	V21, V22, V23, 1, 3	test instruction
000015DE	B98D 0020			928+	EPSW	R2, R0	extract psw
000015E2	5020 500C		0000000C	929+	ST	R2, CCPSW	to save CC
000015E6	E750 5040 080E		000015A8	930+	VST	V21, V107	save v1 output
000015EC	07FB			931+	BR	R11	return
000015F0				932+RE7	DC	0F	V1 for this test
000015F0				933+	DROP	R5	
000015F0	00000000 00000010			934	DC	XL16' 00000000000000010000000000000000'	V1
000015F8	00000000 00000000						
00001600	5D3A5859 5A535953			935	DC	XL16' 5D3A58595A53595354454D445F444546'	v2
00001608	54454D44 5F444546						
00001610	25252525 25252525			936	DC	XL16' 25252525252525252525252525252525'	v3
00001618	25252525 25252525						
				937			
				938	* Halfword, Equal, no zero		cc=1
				939	VRR_B	VFEE, 1, 3, 1	
00001620				940+	DS	0FD	
00001620		00001620		941+	USING	*, R5	base for test data and test routine
00001620	00001678			942+T8	DC	A(X8)	address of test routine



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001624	0008			943+	DC	H' 8' test number
00001626	00			944+	DC	X' 00'
00001627	01			945+	DC	HL1' 1' m4 used
00001628	03			946+	DC	HL1' 3' m5 used
00001629	01			947+	DC	HL1' 1' CC
0000162A	0B			948+	DC	HL1' 11' CC failed mask
0000162C	00000000 00000000			949+	DS	2F extracted PSW after test (has CC)
00001634	FF			950+	DC	X' FF' extracted CC, if test failed
00001635	E5C6C5C5 40404040			951+	DC	CL8' VFEE' instruction name
00001640	000016A8			952+	DC	A(RE8) address of v1 result
00001644	000016B8			953+	DC	A(RE8+16) address of v2 source
00001648	000016C8			954+	DC	A(RE8+32) address of v3 source
0000164C	00000010			955+	DC	A(16) result length
00001650	000016A8			956+REA8	DC	A(RE8) result address
00001658	00000000 00000000			957+	DS	FD gap
00001660	00000000 00000000			958+V108	DS	XL16 V1 output
00001668	00000000 00000000					
00001670	00000000 00000000			959+	DS	FD gap
				960+*		
00001678				961+X8	DS	0F
00001678	E310 5024 0014		00000024	962+	LGF	R1, V2ADDR load v2 source
0000167E	E761 0000 0806		00000000	963+	VL	v22, 0(R1) use v21 to test decoder
00001684	E310 5028 0014		00000028	964+	LGF	R1, V3ADDR load v3 source
0000168A	E771 0000 0806		00000000	965+	VL	v23, 0(R1) use v22 to test decoder
00001690	E756 7030 1E80			966+	VFEE	V21, V22, V23, 1, 3 test instruction
00001696	B98D 0020			967+	EPSW	R2, R0 extract psw
0000169A	5020 500C		0000000C	968+	ST	R2, CCPSW to save CC
0000169E	E750 5040 080E		00001660	969+	VST	V21, V108 save v1 output
000016A4	07FB			970+	BR	R11 return
000016A8				971+RE8	DC	0F V1 for this test
000016A8				972+	DROP	R5
000016A8	00000000 00000006			973	DC	XL16' 00000000000000006000000000000000' V1
000016B0	00000000 00000000					
000016B8	5D3A5859 5A532525			974	DC	XL16' 5D3A58595A53252554454D445F444546' v2
000016C0	54454D44 5F444546					
000016C8	25252525 25252525			975	DC	XL16' 25252525252525252525252525252525' v3
000016D0	25252525 25252525					
				976		
				977	* Halfword, Equal before zero cc=2	
				978	VRR_B VFEE, 1, 3, 2	
000016D8				979+	DS	0FD
000016D8		000016D8		980+	USING	*, R5 base for test data and test routine
000016D8	00001730			981+T9	DC	A(X9) address of test routine
000016DC	0009			982+	DC	H' 9' test number
000016DE	00			983+	DC	X' 00'
000016DF	01			984+	DC	HL1' 1' m4 used
000016E0	03			985+	DC	HL1' 3' m5 used
000016E1	02			986+	DC	HL1' 2' CC
000016E2	0D			987+	DC	HL1' 13' CC failed mask
000016E4	00000000 00000000			988+	DS	2F extracted PSW after test (has CC)
000016EC	FF			989+	DC	X' FF' extracted CC, if test failed
000016ED	E5C6C5C5 40404040			990+	DC	CL8' VFEE' instruction name
000016F8	00001760			991+	DC	A(RE9) address of v1 result
000016FC	00001770			992+	DC	A(RE9+16) address of v2 source
00001700	00001780			993+	DC	A(RE9+32) address of v3 source
00001704	00000010			994+	DC	A(16) result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001708	00001760			995+REA9	DC	A(RE9)	result address
00001710	00000000 00000000			996+	DS	FD	gap
00001718	00000000 00000000			997+V109	DS	XL16	V1 output
00001720	00000000 00000000						
00001728	00000000 00000000			998+	DS	FD	gap
				999+*			
00001730				1000+X9	DS	0F	
00001730	E310 5024 0014		00000024	1001+	LGF	R1, V2ADDR	load v2 source
00001736	E761 0000 0806		00000000	1002+	VL	v22, 0(R1)	use v21 to test decoder
0000173C	E310 5028 0014		00000028	1003+	LGF	R1, V3ADDR	load v3 source
00001742	E771 0000 0806		00000000	1004+	VL	v23, 0(R1)	use v22 to test decoder
00001748	E756 7030 1E80			1005+	VFEE	V21, V22, V23, 1, 3	test instruction
0000174E	B98D 0020			1006+	EPSW	R2, R0	extract psw
00001752	5020 500C		0000000C	1007+	ST	R2, CCPSW	to save CC
00001756	E750 5040 080E		00001718	1008+	VST	V21, V109	save v1 output
0000175C	07FB			1009+	BR	R11	return
00001760				1010+REA9	DC	0F	V1 for this test
00001760				1011+	DROP	R5	
00001760	00000000 00000006			1012	DC	XL16' 00000000000000000600000000000000'	V1
00001768	00000000 00000000						
00001770	5D3A5859 5A532525			1013	DC	XL16' 5D3A58595A532525544500005F444546'	v2
00001778	54450000 5F444546						
00001780	25252525 25252525			1014	DC	XL16' 25252525252525252525252525252525'	v3
00001788	25252525 25252525						
				1015			
				1016 * Halfword, No		equal, no zero	cc=3
				1017	VRR_B	VFEE, 1, 3, 3	
00001790				1018+	DS	0FD	
00001790		00001790		1019+	USING	*, R5	base for test data and test routine
00001790	000017E8			1020+T10	DC	A(X10)	address of test routine
00001794	000A			1021+	DC	H' 10'	test number
00001796	00			1022+	DC	X' 00'	
00001797	01			1023+	DC	HL1' 1'	m4 used
00001798	03			1024+	DC	HL1' 3'	m5 used
00001799	03			1025+	DC	HL1' 3'	CC
0000179A	0E			1026+	DC	HL1' 14'	CC failed mask
0000179C	00000000 00000000			1027+	DS	2F	extracted PSW after test (has CC)
000017A4	FF			1028+	DC	X' FF'	extracted CC, if test failed
000017A5	E5C6C5C5 40404040			1029+	DC	CL8' VFEE'	instruction name
000017B0	00001818			1030+	DC	A(RE10)	address of v1 result
000017B4	00001828			1031+	DC	A(RE10+16)	address of v2 source
000017B8	00001838			1032+	DC	A(RE10+32)	address of v3 source
000017BC	00000010			1033+	DC	A(16)	result length
000017C0	00001818			1034+REA10	DC	A(RE10)	result address
000017C8	00000000 00000000			1035+	DS	FD	gap
000017D0	00000000 00000000			1036+V1010	DS	XL16	V1 output
000017D8	00000000 00000000						
000017E0	00000000 00000000			1037+	DS	FD	gap
				1038+*			
000017E8				1039+X10	DS	0F	
000017E8	E310 5024 0014		00000024	1040+	LGF	R1, V2ADDR	load v2 source
000017EE	E761 0000 0806		00000000	1041+	VL	v22, 0(R1)	use v21 to test decoder
000017F4	E310 5028 0014		00000028	1042+	LGF	R1, V3ADDR	load v3 source
000017FA	E771 0000 0806		00000000	1043+	VL	v23, 0(R1)	use v22 to test decoder
00001800	E756 7030 1E80			1044+	VFEE	V21, V22, V23, 1, 3	test instruction
00001806	B98D 0020			1045+	EPSW	R2, R0	extract psw

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000180A	5020 500C		0000000C	1046+	ST	R2, CCPSW	to save CC
0000180E	E750 5040 080E		000017D0	1047+	VST	V21, V1010	save v1 output
00001814	07FB			1048+	BR	R11	return
00001818				1049+RE10	DC	0F	V1 for this test
00001818				1050+	DROP	R5	
00001818	00000000 00000010			1051	DC	XL16' 00000000000000001000000000000000'	V1
00001820	00000000 00000000						
00001828	5D3A5859 5A535953			1052	DC	XL16' 5D3A58595A53595354454D445F444546'	v2
00001830	54454D44 5F444546						
00001838	25252525 25252525			1053	DC	XL16' 25252525252525252525252525252525'	v3
00001840	25252525 25252525						
				1054			
				1055 *	Halfword, Equal, no zero		cc=1
				1056	VRR_B	VFEE, 1, 3, 1	
00001848				1057+	DS	0FD	
00001848		00001848		1058+	USING	*, R5	base for test data and test routine
00001848	000018A0			1059+T11	DC	A(X11)	address of test routine
0000184C	000B			1060+	DC	H' 11'	test number
0000184E	00			1061+	DC	X' 00'	
0000184F	01			1062+	DC	HL1' 1'	m4 used
00001850	03			1063+	DC	HL1' 3'	m5 used
00001851	01			1064+	DC	HL1' 1'	CC
00001852	0B			1065+	DC	HL1' 11'	CC failed mask
00001854	00000000 00000000			1066+	DS	2F	extracted PSW after test (has CC)
0000185C	FF			1067+	DC	X' FF'	extracted CC, if test failed
0000185D	E5C6C5C5 40404040			1068+	DC	CL8' VFEE'	instruction name
00001868	000018D0			1069+	DC	A(RE11)	address of v1 result
0000186C	000018E0			1070+	DC	A(RE11+16)	address of v2 source
00001870	000018F0			1071+	DC	A(RE11+32)	address of v3 source
00001874	00000010			1072+	DC	A(16)	result length
00001878	000018D0			1073+REA11	DC	A(RE11)	result address
00001880	00000000 00000000			1074+	DS	FD	gap
00001888	00000000 00000000			1075+V1011	DS	XL16	V1 output
00001890	00000000 00000000						
00001898	00000000 00000000			1076+	DS	FD	gap
				1077+*			
000018A0				1078+X11	DS	0F	
000018A0	E310 5024 0014		00000024	1079+	LGF	R1, V2ADDR	load v2 source
000018A6	E761 0000 0806		00000000	1080+	VL	v22, 0(R1)	use v21 to test decoder
000018AC	E310 5028 0014		00000028	1081+	LGF	R1, V3ADDR	load v3 source
000018B2	E771 0000 0806		00000000	1082+	VL	v23, 0(R1)	use v22 to test decoder
000018B8	E756 7030 1E80			1083+	VFEE	V21, V22, V23, 1, 3	test instruction
000018BE	B98D 0020			1084+	EPSW	R2, R0	extract psw
000018C2	5020 500C		0000000C	1085+	ST	R2, CCPSW	to save CC
000018C6	E750 5040 080E		00001888	1086+	VST	V21, V1011	save v1 output
000018CC	07FB			1087+	BR	R11	return
000018D0				1088+RE11	DC	0F	V1 for this test
000018D0				1089+	DROP	R5	
000018D0	00000000 00000006			1090	DC	XL16' 00000000000000000600000000000000'	V1
000018D8	00000000 00000000						
000018E0	5D3A5859 5A532525			1091	DC	XL16' 5D3A58595A53252554454D445F444546'	v2
000018E8	54454D44 5F444546						
000018F0	25252525 25252525			1092	DC	XL16' 25252525252525252525252525252525'	v3
000018F8	25252525 25252525						
				1093			
				1094 *	Halfword, Equal before zero		cc=2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001900				1095	VRR_B VFEE, 1, 3, 2	
00001900		00001900		1096+	DS OFD	
00001900	00001958			1097+	USING *, R5	base for test data and test routine
00001904	000C			1098+T12	DC A(X12)	address of test routine
00001906	00			1099+	DC H' 12'	test number
00001907	01			1100+	DC X' 00'	
00001908	03			1101+	DC HL1' 1'	m4 used
00001909	02			1102+	DC HL1' 3'	m5 used
0000190A	0D			1103+	DC HL1' 2'	CC
0000190C	00000000 00000000			1104+	DC HL1' 13'	CC failed mask
00001914	FF			1105+	DS 2F	extracted PSW after test (has CC)
00001915	E5C6C5C5 40404040			1106+	DC X' FF'	extracted CC, if test failed
00001920	00001988			1107+	DC CL8' VFEE'	instruction name
00001924	00001998			1108+	DC A(RE12)	address of v1 result
00001928	000019A8			1109+	DC A(RE12+16)	address of v2 source
0000192C	00000010			1110+	DC A(RE12+32)	address of v3 source
00001930	00001988			1111+	DC A(16)	result length
00001938	00000000 00000000			1112+REA12	DC A(RE12)	result address
00001940	00000000 00000000			1113+	DS FD	gap
00001948	00000000 00000000			1114+V1012	DS XL16	V1 output
00001950	00000000 00000000			1115+	DS FD	gap
				1116+*		
00001958				1117+X12	DS OF	
00001958	E310 5024 0014		00000024	1118+	LGF R1, V2ADDR	load v2 source
0000195E	E761 0000 0806		00000000	1119+	VL v22, 0(R1)	use v21 to test decoder
00001964	E310 5028 0014		00000028	1120+	LGF R1, V3ADDR	load v3 source
0000196A	E771 0000 0806		00000000	1121+	VL v23, 0(R1)	use v22 to test decoder
00001970	E756 7030 1E80			1122+	VFEE V21, V22, V23, 1, 3	test instruction
00001976	B98D 0020			1123+	EPSW R2, R0	extract psw
0000197A	5020 500C		0000000C	1124+	ST R2, CCPSW	to save CC
0000197E	E750 5040 080E		00001940	1125+	VST V21, V1012	save v1 output
00001984	07FB			1126+	BR R11	return
00001988				1127+RE12	DC OF	V1 for this test
00001988				1128+	DROP R5	
00001988	00000000 00000006			1129	DC XL16' 00000000000000006000000000000000'	V1
00001990	00000000 00000000					
00001998	5D3A5859 5A532525			1130	DC XL16' 5D3A58595A532525544500005F444546'	v2
000019A0	54450000 5F444546					
000019A8	25252525 25252525			1131	DC XL16' 25252525252525252525252525252525'	v3
000019B0	25252525 25252525					
				1132		
				1133 * Halfword, Equal before zero		cc=0
				1134	VRR_B VFEE, 1, 3, 0	
000019B8				1135+	DS OFD	
000019B8		000019B8		1136+	USING *, R5	base for test data and test routine
000019B8	00001A10			1137+T13	DC A(X13)	address of test routine
000019BC	000D			1138+	DC H' 13'	test number
000019BE	00			1139+	DC X' 00'	
000019BF	01			1140+	DC HL1' 1'	m4 used
000019C0	03			1141+	DC HL1' 3'	m5 used
000019C1	00			1142+	DC HL1' 0'	CC
000019C2	07			1143+	DC HL1' 7'	CC failed mask
000019C4	00000000 00000000			1144+	DS 2F	extracted PSW after test (has CC)
000019CC	FF			1145+	DC X' FF'	extracted CC, if test failed
000019CD	E5C6C5C5 40404040			1146+	DC CL8' VFEE'	instruction name



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000019D8	00001A40			1147+	DC	A(RE13) address of v1 result
000019DC	00001A50			1148+	DC	A(RE13+16) address of v2 source
000019E0	00001A60			1149+	DC	A(RE13+32) address of v3 source
000019E4	00000010			1150+	DC	A(16) result length
000019E8	00001A40			1151+REA13	DC	A(RE13) result address
000019F0	00000000 00000000			1152+	DS	FD gap
000019F8	00000000 00000000			1153+V1013	DS	XL16 V1 output
00001A00	00000000 00000000					
00001A08	00000000 00000000			1154+	DS	FD gap
				1155+*		
00001A10				1156+X13	DS	0F
00001A10	E310 5024 0014		00000024	1157+	LGF	R1, V2ADDR load v2 source
00001A16	E761 0000 0806		00000000	1158+	VL	v22, 0(R1) use v21 to test decoder
00001A1C	E310 5028 0014		00000028	1159+	LGF	R1, V3ADDR load v3 source
00001A22	E771 0000 0806		00000000	1160+	VL	v23, 0(R1) use v22 to test decoder
00001A28	E756 7030 1E80			1161+	VFEE	V21, V22, V23, 1, 3 test instruction
00001A2E	B98D 0020			1162+	EPSW	R2, R0 extract psw
00001A32	5020 500C		0000000C	1163+	ST	R2, CCPSW to save CC
00001A36	E750 5040 080E		000019F8	1164+	VST	V21, V1013 save v1 output
00001A3C	07FB			1165+	BR	R11 return
00001A40				1166+RE13	DC	0F V1 for this test
00001A40				1167+	DROP	R5
00001A40	00000000 00000006			1168	DC	XL16' 00000000000000000600000000000000' V1
00001A48	00000000 00000000					
00001A50	5D3A5859 5A530000			1169	DC	XL16' 5D3A58595A530000544525255F444546' v2
00001A58	54452525 5F444546					
00001A60	25252525 25252525			1170	DC	XL16' 25252525252525252525252525252525' v3
00001A68	25252525 25252525					
				1171		
				1172 * Word, No equal, no zero		cc=3
				1173	VRR_B VFEE, 2, 3, 3	
00001A70				1174+	DS	0FD
00001A70		00001A70		1175+	USING	*, R5 base for test data and test routine
00001A70	00001AC8			1176+T14	DC	A(X14) address of test routine
00001A74	000E			1177+	DC	H' 14' test number
00001A76	00			1178+	DC	X' 00'
00001A77	02			1179+	DC	HL1' 2' m4 used
00001A78	03			1180+	DC	HL1' 3' m5 used
00001A79	03			1181+	DC	HL1' 3' CC
00001A7A	0E			1182+	DC	HL1' 14' CC failed mask
00001A7C	00000000 00000000			1183+	DS	2F extracted PSW after test (has CC)
00001A84	FF			1184+	DC	X' FF' extracted CC, if test failed
00001A85	E5C6C5C5 40404040			1185+	DC	CL8' VFEE' instruction name
00001A90	00001AF8			1186+	DC	A(RE14) address of v1 result
00001A94	00001B08			1187+	DC	A(RE14+16) address of v2 source
00001A98	00001B18			1188+	DC	A(RE14+32) address of v3 source
00001A9C	00000010			1189+	DC	A(16) result length
00001AA0	00001AF8			1190+REA14	DC	A(RE14) result address
00001AA8	00000000 00000000			1191+	DS	FD gap
00001AB0	00000000 00000000			1192+V1014	DS	XL16 V1 output
00001AB8	00000000 00000000					
00001AC0	00000000 00000000			1193+	DS	FD gap
				1194+*		
00001AC8				1195+X14	DS	0F
00001AC8	E310 5024 0014		00000024	1196+	LGF	R1, V2ADDR load v2 source
00001ACE	E761 0000 0806		00000000	1197+	VL	v22, 0(R1) use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001AD4	E310 5028 0014		00000028	1198+	LGF	R1, V3ADDR	load v3 source
00001ADA	E771 0000 0806		00000000	1199+	VL	v23, 0(R1)	use v22 to test decoder
00001AE0	E756 7030 2E80			1200+	VFEE	V21, V22, V23, 2, 3	test instruction
00001AE6	B98D 0020			1201+	EPSW	R2, R0	extract psw
00001AEA	5020 500C		0000000C	1202+	ST	R2, CCPSW	to save CC
00001AEE	E750 5040 080E		00001AB0	1203+	VST	V21, V1014	save v1 output
00001AF4	07FB			1204+	BR	R11	return
00001AF8				1205+RE14	DC	0F	V1 for this test
00001AF8				1206+	DROP	R5	
00001AF8	00000000 00000010			1207	DC	XL16' 00000000000000001000000000000000'	V1
00001B00	00000000 00000000						
00001B08	5D3A5859 5A535953			1208	DC	XL16' 5D3A58595A53595354454D445F444546'	v2
00001B10	54454D44 5F444546						
00001B18	25252525 25252525			1209	DC	XL16' 25252525252525252525252525252525'	v3
00001B20	25252525 25252525						
				1210			
				1211 * Word, Equal, no zero			cc=1
				1212	VRR_B	VFEE, 2, 3, 1	
00001B28				1213+	DS	0FD	
00001B28		00001B28		1214+	USING	*, R5	base for test data and test routine
00001B28	00001B80			1215+T15	DC	A(X15)	address of test routine
00001B2C	000F			1216+	DC	H' 15'	test number
00001B2E	00			1217+	DC	X' 00'	
00001B2F	02			1218+	DC	HL1' 2'	m4 used
00001B30	03			1219+	DC	HL1' 3'	m5 used
00001B31	01			1220+	DC	HL1' 1'	CC
00001B32	0B			1221+	DC	HL1' 11'	CC failed mask
00001B34	00000000 00000000			1222+	DS	2F	extracted PSW after test (has CC)
00001B3C	FF			1223+	DC	X' FF'	extracted CC, if test failed
00001B3D	E5C6C5C5 40404040			1224+	DC	CL8' VFEE'	instruction name
00001B48	00001BB0			1225+	DC	A(RE15)	address of v1 result
00001B4C	00001BC0			1226+	DC	A(RE15+16)	address of v2 source
00001B50	00001BD0			1227+	DC	A(RE15+32)	address of v3 source
00001B54	00000010			1228+	DC	A(16)	result length
00001B58	00001BB0			1229+REA15	DC	A(RE15)	result address
00001B60	00000000 00000000			1230+	DS	FD	gap
00001B68	00000000 00000000			1231+V1015	DS	XL16	V1 output
00001B70	00000000 00000000						
00001B78	00000000 00000000			1232+	DS	FD	gap
				1233+*			
00001B80				1234+X15	DS	0F	
00001B80	E310 5024 0014		00000024	1235+	LGF	R1, V2ADDR	load v2 source
00001B86	E761 0000 0806		00000000	1236+	VL	v22, 0(R1)	use v21 to test decoder
00001B8C	E310 5028 0014		00000028	1237+	LGF	R1, V3ADDR	load v3 source
00001B92	E771 0000 0806		00000000	1238+	VL	v23, 0(R1)	use v22 to test decoder
00001B98	E756 7030 2E80			1239+	VFEE	V21, V22, V23, 2, 3	test instruction
00001B9E	B98D 0020			1240+	EPSW	R2, R0	extract psw
00001BA2	5020 500C		0000000C	1241+	ST	R2, CCPSW	to save CC
00001BA6	E750 5040 080E		00001B68	1242+	VST	V21, V1015	save v1 output
00001BAC	07FB			1243+	BR	R11	return
00001BB0				1244+RE15	DC	0F	V1 for this test
00001BB0				1245+	DROP	R5	
00001BB0	00000000 00000004			1246	DC	XL16' 00000000000000004000000000000000'	V1
00001BB8	00000000 00000000						
00001BC0	5D3A5859 25252525			1247	DC	XL16' 5D3A58592525252554454D445F444546'	v2
00001BC8	54454D44 5F444546						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001BD0	25252525 25252525			1248	DC	XL16' 25252525252525252525252525252525'	v3
00001BD8	25252525 25252525						
				1249			
				1250	* Word, Equal before zero	cc=2	
				1251	VRR_B VFEE, 2, 3, 2		
00001BE0				1252+	DS	OFD	
00001BE0		00001BE0		1253+	USING	*, R5	base for test data and test routine
00001BE0	00001C38			1254+T16	DC	A(X16)	address of test routine
00001BE4	0010			1255+	DC	H' 16'	test number
00001BE6	00			1256+	DC	X' 00'	
00001BE7	02			1257+	DC	HL1' 2'	m4 used
00001BE8	03			1258+	DC	HL1' 3'	m5 used
00001BE9	02			1259+	DC	HL1' 2'	CC
00001BEA	0D			1260+	DC	HL1' 13'	CC failed mask
00001BEC	00000000 00000000			1261+	DS	2F	extracted PSW after test (has CC)
00001BF4	FF			1262+	DC	X' FF'	extracted CC, if test failed
00001BF5	E5C6C5C5 40404040			1263+	DC	CL8' VFEE'	instruction name
00001C00	00001C68			1264+	DC	A(RE16)	address of v1 result
00001C04	00001C78			1265+	DC	A(RE16+16)	address of v2 source
00001C08	00001C88			1266+	DC	A(RE16+32)	address of v3 source
00001C0C	00000010			1267+	DC	A(16)	result length
00001C10	00001C68			1268+REA16	DC	A(RE16)	result address
00001C18	00000000 00000000			1269+	DS	FD	gap
00001C20	00000000 00000000			1270+V1016	DS	XL16	V1 output
00001C28	00000000 00000000						
00001C30	00000000 00000000			1271+	DS	FD	gap
				1272+*			
00001C38				1273+X16	DS	OF	
00001C38	E310 5024 0014		00000024	1274+	LGF	R1, V2ADDR	load v2 source
00001C3E	E761 0000 0806		00000000	1275+	VL	v22, 0(R1)	use v21 to test decoder
00001C44	E310 5028 0014		00000028	1276+	LGF	R1, V3ADDR	load v3 source
00001C4A	E771 0000 0806		00000000	1277+	VL	v23, 0(R1)	use v22 to test decoder
00001C50	E756 7030 2E80			1278+	VFEE	V21, V22, V23, 2, 3	test instruction
00001C56	B98D 0020			1279+	EPSW	R2, R0	extract psw
00001C5A	5020 500C		0000000C	1280+	ST	R2, CCPSW	to save CC
00001C5E	E750 5040 080E		00001C20	1281+	VST	V21, V1016	save v1 output
00001C64	07FB			1282+	BR	R11	return
00001C68				1283+RE16	DC	OF	V1 for this test
00001C68				1284+	DROP	R5	
00001C68	00000000 00000004			1285	DC	XL16' 00000000000000004000000000000000'	V1
00001C70	00000000 00000000						
00001C78	5D3A5859 25252525			1286	DC	XL16' 5D3A585925252525000000005F444546'	v2
00001C80	00000000 5F444546						
00001C88	25252525 25252525			1287	DC	XL16' 25252525252525252525252525252525'	v3
00001C90	25252525 25252525						
				1288			
				1289	* Word, Equal before zero	cc=0	
				1290	VRR_B VFEE, 2, 3, 0		
00001C98				1291+	DS	OFD	
00001C98		00001C98		1292+	USING	*, R5	base for test data and test routine
00001C98	00001CF0			1293+T17	DC	A(X17)	address of test routine
00001C9C	0011			1294+	DC	H' 17'	test number
00001C9E	00			1295+	DC	X' 00'	
00001C9F	02			1296+	DC	HL1' 2'	m4 used
00001CA0	03			1297+	DC	HL1' 3'	m5 used
00001CA1	00			1298+	DC	HL1' 0'	CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001CA2	07			1299+	DC	HL1' 7'	CC failed mask
00001CA4	00000000 00000000			1300+	DS	2F	extracted PSW after test (has CC)
00001CAC	FF			1301+	DC	X' FF'	extracted CC, if test failed
00001CAD	E5C6C5C5 40404040			1302+	DC	CL8' VFEE'	instruction name
00001CB8	00001D20			1303+	DC	A(RE17)	address of v1 result
00001CBC	00001D30			1304+	DC	A(RE17+16)	address of v2 source
00001CC0	00001D40			1305+	DC	A(RE17+32)	address of v3 source
00001CC4	00000010			1306+	DC	A(16)	result length
00001CC8	00001D20			1307+REA17	DC	A(RE17)	result address
00001CD0	00000000 00000000			1308+	DS	FD	gap
00001CD8	00000000 00000000			1309+V1017	DS	XL16	V1 output
00001CE0	00000000 00000000						
00001CE8	00000000 00000000			1310+	DS	FD	gap
				1311+*			
00001CF0				1312+X17	DS	0F	
00001CF0	E310 5024 0014		00000024	1313+	LGF	R1, V2ADDR	load v2 source
00001CF6	E761 0000 0806		00000000	1314+	VL	v22, 0(R1)	use v21 to test decoder
00001CFC	E310 5028 0014		00000028	1315+	LGF	R1, V3ADDR	load v3 source
00001D02	E771 0000 0806		00000000	1316+	VL	v23, 0(R1)	use v22 to test decoder
00001D08	E756 7030 2E80			1317+	VFEE	V21, V22, V23, 2, 3	test instruction
00001D0E	B98D 0020			1318+	EPSW	R2, R0	extract psw
00001D12	5020 500C		0000000C	1319+	ST	R2, CCPSW	to save CC
00001D16	E750 5040 080E		00001CD8	1320+	VST	V21, V1017	save v1 output
00001D1C	07FB			1321+	BR	R11	return
00001D20				1322+RE17	DC	0F	V1 for this test
00001D20				1323+	DROP	R5	
00001D20	00000000 00000004			1324	DC	XL16' 00000000000000004000000000000000'	V1
00001D28	00000000 00000000						
00001D30	5D3A5859 00000000			1325	DC	XL16' 5D3A5859000000000252525255F444546'	v2
00001D38	25252525 5F444546						
00001D40	25252525 25252525			1326	DC	XL16' 25252525252525252525252525252525'	v3
00001D48	25252525 25252525						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1328 *-----	
				1329 * VFENE - Vector Find Element Not Equal	
				1330 *-----	
				1331	
				1332 *-----	
				1333 * case 0 - simple debug	CC=1 ZS=0, CS=1
				1334 *-----	
				1335 *	
				1336	VRR_B VFENE, 0, 1, 3
00001D50				1337+	DS OFD
00001D50		00001D50		1338+	USING *, R5
00001D50	00001DA8			1339+T18	DC A(X18)
00001D54	0012			1340+	DC H' 18'
00001D56	00			1341+	DC X' 00'
00001D57	00			1342+	DC HL1' 0'
00001D58	01			1343+	DC HL1' 1'
00001D59	03			1344+	DC HL1' 3'
00001D5A	0E			1345+	DC HL1' 14'
00001D5C	00000000 00000000			1346+	DS 2F
00001D64	FF			1347+	DC X' FF'
00001D65	E5C6C5D5 C5404040			1348+	DC CL8' VFENE'
00001D70	00001DD8			1349+	DC A(RE18)
00001D74	00001DE8			1350+	DC A(RE18+16)
00001D78	00001DF8			1351+	DC A(RE18+32)
00001D7C	00000010			1352+	DC A(16)
00001D80	00001DD8			1353+REA18	DC A(RE18)
00001D88	00000000 00000000			1354+	DS FD
00001D90	00000000 00000000			1355+V1018	DS XL16
00001D98	00000000 00000000				
00001DA0	00000000 00000000			1356+	DS FD
				1357+*	gap
00001DA8				1358+X18	DS OF
00001DA8	E310 5024 0014		00000024	1359+	LGF R1, V2ADDR
00001DAE	E761 0000 0806		00000000	1360+	VL v22, 0(R1)
00001DB4	E310 5028 0014		00000028	1361+	LGF R1, V3ADDR
00001DBA	E771 0000 0806		00000000	1362+	VL v23, 0(R1)
00001DC0	E756 7010 0E81			1363+	VFENE V21, V22, V23, 0, 1
00001DC6	B98D 0020			1364+	EPSW R2, R0
00001DCA	5020 500C		0000000C	1365+	ST R2, CCPSW
00001DCE	E750 5040 080E		00001D90	1366+	VST V21, V1018
00001DD4	07FB			1367+	BR R11
00001DD8				1368+RE18	DC OF
00001DD8				1369+	DROP R5
00001DD8	00000000 00000010			1370	DC XL16' 00000000000000001000000000000000' V1
00001DE0	00000000 00000000				
00001DE8	00000000 00000000			1371	DC XL16' 00000000000000000000000000000000' v2
00001DF0	00000000 00000000				
00001DF8	00000000 00000000			1372	DC XL16' 00000000000000000000000000000000' v3
00001E00	00000000 00000000				
				1373	
				1374 *-----	
				1375 * case 1 - Hardware Verified	
				1376 *-----	
				1377 * Byte, All equal, no zero	cc=3
				1378	VRR_B VFENE, 0, 3, 3
00001E08				1379+	DS OFD

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001E08		00001E08		1380+	USING *, R5	base for test data and test routine
00001E08	00001E60			1381+T19	DC A(X19)	address of test routine
00001E0C	0013			1382+	DC H' 19'	test number
00001E0E	00			1383+	DC X' 00'	
00001E0F	00			1384+	DC HL1' 0'	m4 used
00001E10	03			1385+	DC HL1' 3'	m5 used
00001E11	03			1386+	DC HL1' 3'	CC
00001E12	0E			1387+	DC HL1' 14'	CC failed mask
00001E14	00000000 00000000			1388+	DS 2F	extracted PSW after test (has CC)
00001E1C	FF			1389+	DC X' FF'	extracted CC, if test failed
00001E1D	E5C6C5D5 C5404040			1390+	DC CL8' VFENE'	instruction name
00001E28	00001E90			1391+	DC A(RE19)	address of v1 result
00001E2C	00001EA0			1392+	DC A(RE19+16)	address of v2 source
00001E30	00001EB0			1393+	DC A(RE19+32)	address of v3 source
00001E34	00000010			1394+	DC A(16)	result length
00001E38	00001E90			1395+REA19	DC A(RE19)	result address
00001E40	00000000 00000000			1396+	DS FD	gap
00001E48	00000000 00000000			1397+V1019	DS XL16	V1 output
00001E50	00000000 00000000					
00001E58	00000000 00000000			1398+	DS FD	gap
				1399+*		
00001E60				1400+X19	DS 0F	
00001E60	E310 5024 0014		00000024	1401+	LGF R1, V2ADDR	load v2 source
00001E66	E761 0000 0806		00000000	1402+	VL v22, 0(R1)	use v21 to test decoder
00001E6C	E310 5028 0014		00000028	1403+	LGF R1, V3ADDR	load v3 source
00001E72	E771 0000 0806		00000000	1404+	VL v23, 0(R1)	use v22 to test decoder
00001E78	E756 7030 0E81			1405+	VFENE V21, V22, V23, 0, 3	test instruction
00001E7E	B98D 0020			1406+	EPSW R2, R0	extract psw
00001E82	5020 500C		0000000C	1407+	ST R2, CCPSW	to save CC
00001E86	E750 5040 080E		00001E48	1408+	VST V21, V1019	save v1 output
00001E8C	07FB			1409+	BR R11	return
00001E90				1410+RE19	DC 0F	V1 for this test
00001E90				1411+	DROP R5	
00001E90	00000000 00000010			1412	DC XL16' 00000000000000001000000000000000'	V1
00001E98	00000000 00000000					
00001EA0	5D3A5859 5A535953			1413	DC XL16' 5D3A58595A53595354454D445F444546'	v2
00001EA8	54454D44 5F444546					
00001EB0	5D3A5859 5A535953			1414	DC XL16' 5D3A58595A53595354454D445F444546'	v3
00001EB8	54454D44 5F444546					
				1415		
				1416 * Byte, All equal, with zero		cc=0
				1417	VRR_B VFENE, 0, 3, 0	
00001EC0				1418+	DS 0FD	
00001EC0		00001EC0		1419+	USING *, R5	base for test data and test routine
00001EC0	00001F18			1420+T20	DC A(X20)	address of test routine
00001EC4	0014			1421+	DC H' 20'	test number
00001EC6	00			1422+	DC X' 00'	
00001EC7	00			1423+	DC HL1' 0'	m4 used
00001EC8	03			1424+	DC HL1' 3'	m5 used
00001EC9	00			1425+	DC HL1' 0'	CC
00001ECA	07			1426+	DC HL1' 7'	CC failed mask
00001ECC	00000000 00000000			1427+	DS 2F	extracted PSW after test (has CC)
00001ED4	FF			1428+	DC X' FF'	extracted CC, if test failed
00001ED5	E5C6C5D5 C5404040			1429+	DC CL8' VFENE'	instruction name
00001EE0	00001F48			1430+	DC A(RE20)	address of v1 result
00001EE4	00001F58			1431+	DC A(RE20+16)	address of v2 source



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001EE8	00001F68			1432+	DC	A(RE20+32)	address of v3 source
00001EEC	00000010			1433+	DC	A(16)	result length
00001EF0	00001F48			1434+REA20	DC	A(RE20)	result address
00001EF8	00000000 00000000			1435+	DS	FD	gap
00001F00	00000000 00000000			1436+V1020	DS	XL16	V1 output
00001F08	00000000 00000000						
00001F10	00000000 00000000			1437+	DS	FD	gap
				1438+*			
00001F18				1439+X20	DS	0F	
00001F18	E310 5024 0014		00000024	1440+	LGF	R1, V2ADDR	load v2 source
00001F1E	E761 0000 0806		00000000	1441+	VL	v22, 0(R1)	use v21 to test decoder
00001F24	E310 5028 0014		00000028	1442+	LGF	R1, V3ADDR	load v3 source
00001F2A	E771 0000 0806		00000000	1443+	VL	v23, 0(R1)	use v22 to test decoder
00001F30	E756 7030 0E81			1444+	VFENE	V21, V22, V23, 0, 3	test instruction
00001F36	B98D 0020			1445+	EPSW	R2, R0	extract psw
00001F3A	5020 500C		0000000C	1446+	ST	R2, CCPSW	to save CC
00001F3E	E750 5040 080E		00001F00	1447+	VST	V21, V1020	save v1 output
00001F44	07FB			1448+	BR	R11	return
00001F48				1449+RE20	DC	0F	V1 for this test
00001F48				1450+	DROP	R5	
00001F48	00000000 00000009			1451	DC	XL16' 00000000000000009000000000000000'	V1
00001F50	00000000 00000000						
00001F58	5D3A5859 5A535953			1452	DC	XL16' 5D3A58595A53595354004D445F444546'	v2
00001F60	54004D44 5F444546						
00001F68	5D3A5859 5A535953			1453	DC	XL16' 5D3A58595A53595354004D445F444546'	v3
00001F70	54004D44 5F444546						
				1454			
				1455 * Byte, Not Equal, no zero			cc=1
				1456	VRR_B	VFENE, 0, 3, 1	
00001F78				1457+	DS	0FD	
00001F78		00001F78		1458+	USING	*, R5	base for test data and test routine
00001F78	00001FD0			1459+T21	DC	A(X21)	address of test routine
00001F7C	0015			1460+	DC	H' 21'	test number
00001F7E	00			1461+	DC	X' 00'	
00001F7F	00			1462+	DC	HL1' 0'	m4 used
00001F80	03			1463+	DC	HL1' 3'	m5 used
00001F81	01			1464+	DC	HL1' 1'	CC
00001F82	0B			1465+	DC	HL1' 11'	CC failed mask
00001F84	00000000 00000000			1466+	DS	2F	extracted PSW after test (has CC)
00001F8C	FF			1467+	DC	X' FF'	extracted CC, if test failed
00001F8D	E5C6C5D5 C5404040			1468+	DC	CL8' VFENE'	instruction name
00001F98	00002000			1469+	DC	A(RE21)	address of v1 result
00001F9C	00002010			1470+	DC	A(RE21+16)	address of v2 source
00001FA0	00002020			1471+	DC	A(RE21+32)	address of v3 source
00001FA4	00000010			1472+	DC	A(16)	result length
00001FA8	00002000			1473+REA21	DC	A(RE21)	result address
00001FB0	00000000 00000000			1474+	DS	FD	gap
00001FB8	00000000 00000000			1475+V1021	DS	XL16	V1 output
00001FC0	00000000 00000000						
00001FC8	00000000 00000000			1476+	DS	FD	gap
				1477+*			
00001FD0				1478+X21	DS	0F	
00001FD0	E310 5024 0014		00000024	1479+	LGF	R1, V2ADDR	load v2 source
00001FD6	E761 0000 0806		00000000	1480+	VL	v22, 0(R1)	use v21 to test decoder
00001FDC	E310 5028 0014		00000028	1481+	LGF	R1, V3ADDR	load v3 source
00001FE2	E771 0000 0806		00000000	1482+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001FE8	E756 7030 0E81			1483+	VFENE	V21, V22, V23, 0, 3	test instruction
00001FEE	B98D 0020			1484+	EPSW	R2, R0	extract psw
00001FF2	5020 500C		0000000C	1485+	ST	R2, CCPSW	to save CC
00001FF6	E750 5040 080E		00001FB8	1486+	VST	V21, V1021	save v1 output
00001FFC	07FB			1487+	BR	R11	return
00002000				1488+RE21	DC	0F	V1 for this test
00002000				1489+	DROP	R5	
00002000	00000000 00000005			1490	DC	XL16' 00000000000000005000000000000000'	V1
00002008	00000000 00000000						
00002010	5D3A5859 5A255953			1491	DC	XL16' 5D3A58595A25595354454D445F444546'	v2
00002018	54454D44 5F444546						
00002020	5D3A5859 5A535953			1492	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
00002028	54454D44 5F444546						
				1493			
				1494 * Byte, Not Equal before zero			cc=1
				1495	VRR_B	VFENE, 0, 3, 1	
00002030				1496+	DS	0FD	
00002030		00002030		1497+	USING	*, R5	base for test data and test routine
00002030	00002088			1498+T22	DC	A(X22)	address of test routine
00002034	0016			1499+	DC	H' 22'	test number
00002036	00			1500+	DC	X' 00'	
00002037	00			1501+	DC	HL1' 0'	m4 used
00002038	03			1502+	DC	HL1' 3'	m5 used
00002039	01			1503+	DC	HL1' 1'	CC
0000203A	0B			1504+	DC	HL1' 11'	CC failed mask
0000203C	00000000 00000000			1505+	DS	2F	extracted PSW after test (has CC)
00002044	FF			1506+	DC	X' FF'	extracted CC, if test failed
00002045	E5C6C5D5 C5404040			1507+	DC	CL8' VFENE'	instruction name
00002050	000020B8			1508+	DC	A(RE22)	address of v1 result
00002054	000020C8			1509+	DC	A(RE22+16)	address of v2 source
00002058	000020D8			1510+	DC	A(RE22+32)	address of v3 source
0000205C	00000010			1511+	DC	A(16)	result length
00002060	000020B8			1512+REA22	DC	A(RE22)	result address
00002068	00000000 00000000			1513+	DS	FD	gap
00002070	00000000 00000000			1514+V1022	DS	XL16	V1 output
00002078	00000000 00000000						
00002080	00000000 00000000			1515+	DS	FD	gap
				1516+*			
00002088				1517+X22	DS	0F	
00002088	E310 5024 0014		00000024	1518+	LGF	R1, V2ADDR	load v2 source
0000208E	E761 0000 0806		00000000	1519+	VL	v22, 0(R1)	use v21 to test decoder
00002094	E310 5028 0014		00000028	1520+	LGF	R1, V3ADDR	load v3 source
0000209A	E771 0000 0806		00000000	1521+	VL	v23, 0(R1)	use v22 to test decoder
000020A0	E756 7030 0E81			1522+	VFENE	V21, V22, V23, 0, 3	test instruction
000020A6	B98D 0020			1523+	EPSW	R2, R0	extract psw
000020AA	5020 500C		0000000C	1524+	ST	R2, CCPSW	to save CC
000020AE	E750 5040 080E		00002070	1525+	VST	V21, V1022	save v1 output
000020B4	07FB			1526+	BR	R11	return
000020B8				1527+RE22	DC	0F	V1 for this test
000020B8				1528+	DROP	R5	
000020B8	00000000 00000005			1529	DC	XL16' 00000000000000005000000000000000'	V1
000020C0	00000000 00000000						
000020C8	5D3A5859 5A255953			1530	DC	XL16' 5D3A58595A25595354004D445F444546'	v2
000020D0	54004D44 5F444546						
000020D8	5D3A5859 5A535953			1531	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
000020E0	54454D44 5F444546						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1532	
				1533 * Byte, Not Equal after zero	cc=1
				1534 VRR_B VFENE, 0, 3, 1	
000020E8				1535+ DS OFD	
000020E8		000020E8		1536+ USING *, R5	base for test data and test routine
000020E8	00002140			1537+T23 DC A(X23)	address of test routine
000020EC	0017			1538+ DC H' 23'	test number
000020EE	00			1539+ DC X' 00'	
000020EF	00			1540+ DC HL1' 0'	m4 used
000020F0	03			1541+ DC HL1' 3'	m5 used
000020F1	01			1542+ DC HL1' 1'	CC
000020F2	0B			1543+ DC HL1' 11'	CC failed mask
000020F4	00000000 00000000			1544+ DS 2F	extracted PSW after test (has CC)
000020FC	FF			1545+ DC X' FF'	extracted CC, if test failed
000020FD	E5C6C5D5 C5404040			1546+ DC CL8' VFENE'	instruction name
00002108	00002170			1547+ DC A(RE23)	address of v1 result
0000210C	00002180			1548+ DC A(RE23+16)	address of v2 source
00002110	00002190			1549+ DC A(RE23+32)	address of v3 source
00002114	00000010			1550+ DC A(16)	result length
00002118	00002170			1551+REA23 DC A(RE23)	result address
00002120	00000000 00000000			1552+ DS FD	gap
00002128	00000000 00000000			1553+V1023 DS XL16	V1 output
00002130	00000000 00000000				
00002138	00000000 00000000			1554+ DS FD	gap
				1555+*	
00002140				1556+X23 DS OF	
00002140	E310 5024 0014		00000024	1557+ LGF R1, V2ADDR	load v2 source
00002146	E761 0000 0806		00000000	1558+ VL v22, 0(R1)	use v21 to test decoder
0000214C	E310 5028 0014		00000028	1559+ LGF R1, V3ADDR	load v3 source
00002152	E771 0000 0806		00000000	1560+ VL v23, 0(R1)	use v22 to test decoder
00002158	E756 7030 0E81			1561+ VFENE V21, V22, V23, 0, 3	test instruction
0000215E	B98D 0020			1562+ EPSW R2, R0	extract psw
00002162	5020 500C		0000000C	1563+ ST R2, CCPSW	to save CC
00002166	E750 5040 080E		00002128	1564+ VST V21, V1023	save v1 output
0000216C	07FB			1565+ BR R11	return
00002170				1566+RE23 DC OF	V1 for this test
00002170				1567+ DROP R5	
00002170	00000000 00000005			1568 DC XL16' 00000000000000005000000000000000'	V1
00002178	00000000 00000000				
00002180	5D3A5859 5A005953			1569 DC XL16' 5D3A58595A00595354254D445F444546'	v2
00002188	54254D44 5F444546				
00002190	5D3A5859 5A535953			1570 DC XL16' 5D3A58595A53595354454D445F444546'	v3
00002198	54454D44 5F444546				
				1571	
				1572 * Halfword, All equal, no zero	cc=3
				1573 VRR_B VFENE, 1, 3, 3	
000021A0				1574+ DS OFD	
000021A0		000021A0		1575+ USING *, R5	base for test data and test routine
000021A0	000021F8			1576+T24 DC A(X24)	address of test routine
000021A4	0018			1577+ DC H' 24'	test number
000021A6	00			1578+ DC X' 00'	
000021A7	01			1579+ DC HL1' 1'	m4 used
000021A8	03			1580+ DC HL1' 3'	m5 used
000021A9	03			1581+ DC HL1' 3'	CC
000021AA	0E			1582+ DC HL1' 14'	CC failed mask
000021AC	00000000 00000000			1583+ DS 2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000021B4	FF			1584+	DC	X' FF'	extracted CC, if test failed
000021B5	E5C6C5D5 C5404040			1585+	DC	CL8' VFENE'	instruction name
000021C0	00002228			1586+	DC	A(RE24)	address of v1 result
000021C4	00002238			1587+	DC	A(RE24+16)	address of v2 source
000021C8	00002248			1588+	DC	A(RE24+32)	address of v3 source
000021CC	00000010			1589+	DC	A(16)	result length
000021D0	00002228			1590+REA24	DC	A(RE24)	result address
000021D8	00000000 00000000			1591+	DS	FD	gap
000021E0	00000000 00000000			1592+V1024	DS	XL16	V1 output
000021E8	00000000 00000000						
000021F0	00000000 00000000			1593+	DS	FD	gap
				1594+*			
000021F8				1595+X24	DS	0F	
000021F8	E310 5024 0014		00000024	1596+	LGF	R1, V2ADDR	load v2 source
000021FE	E761 0000 0806		00000000	1597+	VL	v22, 0(R1)	use v21 to test decoder
00002204	E310 5028 0014		00000028	1598+	LGF	R1, V3ADDR	load v3 source
0000220A	E771 0000 0806		00000000	1599+	VL	v23, 0(R1)	use v22 to test decoder
00002210	E756 7030 1E81			1600+	VFENE	V21, V22, V23, 1, 3	test instruction
00002216	B98D 0020			1601+	EPSW	R2, R0	extract psw
0000221A	5020 500C		0000000C	1602+	ST	R2, CCPSW	to save CC
0000221E	E750 5040 080E		000021E0	1603+	VST	V21, V1024	save v1 output
00002224	07FB			1604+	BR	R11	return
00002228				1605+RE24	DC	0F	V1 for this test
00002228				1606+	DROP	R5	
00002228	00000000 00000010			1607	DC	XL16' 00000000000000001000000000000000'	V1
00002230	00000000 00000000						
00002238	5D3A5859 5A535953			1608	DC	XL16' 5D3A58595A53595354454D445F444546'	v2
00002240	54454D44 5F444546						
00002248	5D3A5859 5A535953			1609	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
00002250	54454D44 5F444546						
				1610			
				1611 * Halfword, Not Equal, no zero		cc=1	
				1612	VRR_B	VFENE, 1, 3, 1	
00002258				1613+	DS	0FD	
00002258		00002258		1614+	USING	*, R5	base for test data and test routine
00002258	000022B0			1615+T25	DC	A(X25)	address of test routine
0000225C	0019			1616+	DC	H' 25'	test number
0000225E	00			1617+	DC	X' 00'	
0000225F	01			1618+	DC	HL1' 1'	m4 used
00002260	03			1619+	DC	HL1' 3'	m5 used
00002261	01			1620+	DC	HL1' 1'	CC
00002262	0B			1621+	DC	HL1' 11'	CC failed mask
00002264	00000000 00000000			1622+	DS	2F	extracted PSW after test (has CC)
0000226C	FF			1623+	DC	X' FF'	extracted CC, if test failed
0000226D	E5C6C5D5 C5404040			1624+	DC	CL8' VFENE'	instruction name
00002278	000022E0			1625+	DC	A(RE25)	address of v1 result
0000227C	000022F0			1626+	DC	A(RE25+16)	address of v2 source
00002280	00002300			1627+	DC	A(RE25+32)	address of v3 source
00002284	00000010			1628+	DC	A(16)	result length
00002288	000022E0			1629+REA25	DC	A(RE25)	result address
00002290	00000000 00000000			1630+	DS	FD	gap
00002298	00000000 00000000			1631+V1025	DS	XL16	V1 output
000022A0	00000000 00000000						
000022A8	00000000 00000000			1632+	DS	FD	gap
				1633+*			
000022B0				1634+X25	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000022B0	E310 5024 0014		00000024	1635+	LGF	R1, V2ADDR	load v2 source
000022B6	E761 0000 0806		00000000	1636+	VL	v22, 0(R1)	use v21 to test decoder
000022BC	E310 5028 0014		00000028	1637+	LGF	R1, V3ADDR	load v3 source
000022C2	E771 0000 0806		00000000	1638+	VL	v23, 0(R1)	use v22 to test decoder
000022C8	E756 7030 1E81			1639+	VFENE	V21, V22, V23, 1, 3	test instruction
000022CE	B98D 0020			1640+	EPSW	R2, R0	extract psw
000022D2	5020 500C		0000000C	1641+	ST	R2, CCPSW	to save CC
000022D6	E750 5040 080E		00002298	1642+	VST	V21, V1025	save v1 output
000022DC	07FB			1643+	BR	R11	return
000022E0				1644+RE25	DC	0F	V1 for this test
000022E0				1645+	DROP	R5	
000022E0	00000000 00000006			1646	DC	XL16' 0000000000000000060000000000000000'	V1
000022E8	00000000 00000000						
000022F0	5D3A5859 5A532525			1647	DC	XL16' 5D3A58595A53252554454D445F444546'	v2
000022F8	54454D44 5F444546						
00002300	5D3A5859 5A535953			1648	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
00002308	54454D44 5F444546						
				1649			
				1650 *	Halfword, Not Equal before zero	cc=1	
				1651	VRR_B	VFENE, 1, 3, 1	
00002310				1652+	DS	0FD	
00002310		00002310		1653+	USING	*, R5	base for test data and test routine
00002310	00002368			1654+T26	DC	A(X26)	address of test routine
00002314	001A			1655+	DC	H' 26'	test number
00002316	00			1656+	DC	X' 00'	
00002317	01			1657+	DC	HL1' 1'	m4 used
00002318	03			1658+	DC	HL1' 3'	m5 used
00002319	01			1659+	DC	HL1' 1'	CC
0000231A	0B			1660+	DC	HL1' 11'	CC failed mask
0000231C	00000000 00000000			1661+	DS	2F	extracted PSW after test (has CC)
00002324	FF			1662+	DC	X' FF'	extracted CC, if test failed
00002325	E5C6C5D5 C5404040			1663+	DC	CL8' VFENE'	instruction name
00002330	00002398			1664+	DC	A(RE26)	address of v1 result
00002334	000023A8			1665+	DC	A(RE26+16)	address of v2 source
00002338	000023B8			1666+	DC	A(RE26+32)	address of v3 source
0000233C	00000010			1667+	DC	A(16)	result length
00002340	00002398			1668+REA26	DC	A(RE26)	result address
00002348	00000000 00000000			1669+	DS	FD	gap
00002350	00000000 00000000			1670+V1026	DS	XL16	V1 output
00002358	00000000 00000000						
00002360	00000000 00000000			1671+	DS	FD	gap
				1672+*			
00002368				1673+X26	DS	0F	
00002368	E310 5024 0014		00000024	1674+	LGF	R1, V2ADDR	load v2 source
0000236E	E761 0000 0806		00000000	1675+	VL	v22, 0(R1)	use v21 to test decoder
00002374	E310 5028 0014		00000028	1676+	LGF	R1, V3ADDR	load v3 source
0000237A	E771 0000 0806		00000000	1677+	VL	v23, 0(R1)	use v22 to test decoder
00002380	E756 7030 1E81			1678+	VFENE	V21, V22, V23, 1, 3	test instruction
00002386	B98D 0020			1679+	EPSW	R2, R0	extract psw
0000238A	5020 500C		0000000C	1680+	ST	R2, CCPSW	to save CC
0000238E	E750 5040 080E		00002350	1681+	VST	V21, V1026	save v1 output
00002394	07FB			1682+	BR	R11	return
00002398				1683+RE26	DC	0F	V1 for this test
00002398				1684+	DROP	R5	
00002398	00000000 00000006			1685	DC	XL16' 0000000000000000060000000000000000'	V1
000023A0	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000023A8	5D3A5859 5A532525			1686	DC	XL16' 5D3A58595A532525544500005F444546'	v2
000023B0	54450000 5F444546						
000023B8	5D3A5859 5A535953			1687	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
000023C0	54454D44 5F444546						
				1688			
				1689	* Halfword, Not Equal after zero		cc=1
				1690	VRR_B VFENE, 1, 3, 1		
000023C8				1691+	DS	OFD	
000023C8		000023C8		1692+	USING	*, R5	base for test data and test routine
000023C8	00002420			1693+T27	DC	A(X27)	address of test routine
000023CC	001B			1694+	DC	H' 27'	test number
000023CE	00			1695+	DC	X' 00'	
000023CF	01			1696+	DC	HL1' 1'	m4 used
000023D0	03			1697+	DC	HL1' 3'	m5 used
000023D1	01			1698+	DC	HL1' 1'	CC
000023D2	0B			1699+	DC	HL1' 11'	CC failed mask
000023D4	00000000 00000000			1700+	DS	2F	extracted PSW after test (has CC)
000023DC	FF			1701+	DC	X' FF'	extracted CC, if test failed
000023DD	E5C6C5D5 C5404040			1702+	DC	CL8' VFENE'	instruction name
000023E8	00002450			1703+	DC	A(RE27)	address of v1 result
000023EC	00002460			1704+	DC	A(RE27+16)	address of v2 source
000023F0	00002470			1705+	DC	A(RE27+32)	address of v3 source
000023F4	00000010			1706+	DC	A(16)	result length
000023F8	00002450			1707+REA27	DC	A(RE27)	result address
00002400	00000000 00000000			1708+	DS	FD	gap
00002408	00000000 00000000			1709+V1027	DS	XL16	V1 output
00002410	00000000 00000000						
00002418	00000000 00000000			1710+	DS	FD	gap
				1711+*			
00002420				1712+X27	DS	OF	
00002420	E310 5024 0014		00000024	1713+	LGF	R1, V2ADDR	load v2 source
00002426	E761 0000 0806		00000000	1714+	VL	v22, 0(R1)	use v21 to test decoder
0000242C	E310 5028 0014		00000028	1715+	LGF	R1, V3ADDR	load v3 source
00002432	E771 0000 0806		00000000	1716+	VL	v23, 0(R1)	use v22 to test decoder
00002438	E756 7030 1E81			1717+	VFENE	V21, V22, V23, 1, 3	test instruction
0000243E	B98D 0020			1718+	EPSW	R2, R0	extract psw
00002442	5020 500C		0000000C	1719+	ST	R2, CCPSW	to save CC
00002446	E750 5040 080E		00002408	1720+	VST	V21, V1027	save v1 output
0000244C	07FB			1721+	BR	R11	return
00002450				1722+RE27	DC	OF	V1 for this test
00002450				1723+	DROP	R5	
00002450	00000000 00000006			1724	DC	XL16' 00000000000000006000000000000000'	V1
00002458	00000000 00000000						
00002460	5D3A5859 5A530000			1725	DC	XL16' 5D3A58595A530000544525255F444546'	v2
00002468	54452525 5F444546						
00002470	5D3A5859 5A535953			1726	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
00002478	54454D44 5F444546						
				1727			
				1728	* Word, All equal, no zero		cc=3
				1729	VRR_B VFENE, 2, 3, 3		
00002480				1730+	DS	OFD	
00002480		00002480		1731+	USING	*, R5	base for test data and test routine
00002480	000024D8			1732+T28	DC	A(X28)	address of test routine
00002484	001C			1733+	DC	H' 28'	test number
00002486	00			1734+	DC	X' 00'	
00002487	02			1735+	DC	HL1' 2'	m4 used



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002488	03			1736+	DC	HL1' 3' m5 used
00002489	03			1737+	DC	HL1' 3' CC
0000248A	0E			1738+	DC	HL1' 14' CC failed mask
0000248C	00000000 00000000			1739+	DS	2F extracted PSW after test (has CC)
00002494	FF			1740+	DC	X' FF' extracted CC, if test failed
00002495	E5C6C5D5 C5404040			1741+	DC	CL8' VFENE' instruction name
000024A0	00002508			1742+	DC	A(RE28) address of v1 result
000024A4	00002518			1743+	DC	A(RE28+16) address of v2 source
000024A8	00002528			1744+	DC	A(RE28+32) address of v3 source
000024AC	00000010			1745+	DC	A(16) result length
000024B0	00002508			1746+REA28	DC	A(RE28) result address
000024B8	00000000 00000000			1747+	DS	FD gap
000024C0	00000000 00000000			1748+V1028	DS	XL16 V1 output
000024C8	00000000 00000000					
000024D0	00000000 00000000			1749+	DS	FD gap
				1750+*		
000024D8				1751+X28	DS	0F
000024D8	E310 5024 0014		00000024	1752+	LGF	R1, V2ADDR load v2 source
000024DE	E761 0000 0806		00000000	1753+	VL	v22, 0(R1) use v21 to test decoder
000024E4	E310 5028 0014		00000028	1754+	LGF	R1, V3ADDR load v3 source
000024EA	E771 0000 0806		00000000	1755+	VL	v23, 0(R1) use v22 to test decoder
000024F0	E756 7030 2E81			1756+	VFENE	V21, V22, V23, 2, 3 test instruction
000024F6	B98D 0020			1757+	EPSW	R2, R0 extract psw
000024FA	5020 500C		0000000C	1758+	ST	R2, CCPSW to save CC
000024FE	E750 5040 080E		000024C0	1759+	VST	V21, V1028 save v1 output
00002504	07FB			1760+	BR	R11 return
00002508				1761+RE28	DC	0F V1 for this test
00002508				1762+	DROP	R5
00002508	00000000 00000010			1763	DC	XL16' 00000000000000001000000000000000' V1
00002510	00000000 00000000					
00002518	5D3A5859 5A535953			1764	DC	XL16' 5D3A58595A53595354454D445F444546' v2
00002520	54454D44 5F444546					
00002528	5D3A5859 5A535953			1765	DC	XL16' 5D3A58595A53595354454D445F444546' v3
00002530	54454D44 5F444546					
				1766		
				1767 * Word, Not Equal, no zero		cc=1
				1768	VRR_B	VFENE, 2, 3, 1
00002538				1769+	DS	0FD
00002538		00002538		1770+	USING	*, R5 base for test data and test routine
00002538	00002590			1771+T29	DC	A(X29) address of test routine
0000253C	001D			1772+	DC	H' 29' test number
0000253E	00			1773+	DC	X' 00'
0000253F	02			1774+	DC	HL1' 2' m4 used
00002540	03			1775+	DC	HL1' 3' m5 used
00002541	01			1776+	DC	HL1' 1' CC
00002542	0B			1777+	DC	HL1' 11' CC failed mask
00002544	00000000 00000000			1778+	DS	2F extracted PSW after test (has CC)
0000254C	FF			1779+	DC	X' FF' extracted CC, if test failed
0000254D	E5C6C5D5 C5404040			1780+	DC	CL8' VFENE' instruction name
00002558	000025C0			1781+	DC	A(RE29) address of v1 result
0000255C	000025D0			1782+	DC	A(RE29+16) address of v2 source
00002560	000025E0			1783+	DC	A(RE29+32) address of v3 source
00002564	00000010			1784+	DC	A(16) result length
00002568	000025C0			1785+REA29	DC	A(RE29) result address
00002570	00000000 00000000			1786+	DS	FD gap
00002578	00000000 00000000			1787+V1029	DS	XL16 V1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002580	00000000 00000000						
00002588	00000000 00000000			1788+	DS	FD	gap
				1789+*			
00002590				1790+X29	DS	OF	
00002590	E310 5024 0014		00000024	1791+	LGF	R1, V2ADDR	load v2 source
00002596	E761 0000 0806		00000000	1792+	VL	v22, 0(R1)	use v21 to test decoder
0000259C	E310 5028 0014		00000028	1793+	LGF	R1, V3ADDR	load v3 source
000025A2	E771 0000 0806		00000000	1794+	VL	v23, 0(R1)	use v22 to test decoder
000025A8	E756 7030 2E81			1795+	VFENE	V21, V22, V23, 2, 3	test instruction
000025AE	B98D 0020			1796+	EPSW	R2, R0	extract psw
000025B2	5020 500C		0000000C	1797+	ST	R2, CCPSW	to save CC
000025B6	E750 5040 080E		00002578	1798+	VST	V21, V1029	save v1 output
000025BC	07FB			1799+	BR	R11	return
000025C0				1800+RE29	DC	OF	V1 for this test
000025C0				1801+	DROP	R5	
000025C0	00000000 00000004			1802	DC	XL16' 00000000000000004000000000000000'	V1
000025C8	00000000 00000000						
000025D0	5D3A5859 25252525			1803	DC	XL16' 5D3A58592525252554454D445F444546'	v2
000025D8	54454D44 5F444546						
000025E0	5D3A5859 5A535953			1804	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
000025E8	54454D44 5F444546						
				1805			
				1806 * Word, Not Equal before zero			cc=1
				1807	VRR_B	VFENE, 2, 3, 1	
000025F0				1808+	DS	OFD	
000025F0		000025F0		1809+	USING	*, R5	base for test data and test routine
000025F0	00002648			1810+T30	DC	A(X30)	address of test routine
000025F4	001E			1811+	DC	H' 30'	test number
000025F6	00			1812+	DC	X' 00'	
000025F7	02			1813+	DC	HL1' 2'	m4 used
000025F8	03			1814+	DC	HL1' 3'	m5 used
000025F9	01			1815+	DC	HL1' 1'	CC
000025FA	0B			1816+	DC	HL1' 11'	CC failed mask
000025FC	00000000 00000000			1817+	DS	2F	extracted PSW after test (has CC)
00002604	FF			1818+	DC	X' FF'	extracted CC, if test failed
00002605	E5C6C5D5 C5404040			1819+	DC	CL8' VFENE'	instruction name
00002610	00002678			1820+	DC	A(RE30)	address of v1 result
00002614	00002688			1821+	DC	A(RE30+16)	address of v2 source
00002618	00002698			1822+	DC	A(RE30+32)	address of v3 source
0000261C	00000010			1823+	DC	A(16)	result length
00002620	00002678			1824+REA30	DC	A(RE30)	result address
00002628	00000000 00000000			1825+	DS	FD	gap
00002630	00000000 00000000			1826+V1030	DS	XL16	V1 output
00002638	00000000 00000000						
00002640	00000000 00000000			1827+	DS	FD	gap
				1828+*			
00002648				1829+X30	DS	OF	
00002648	E310 5024 0014		00000024	1830+	LGF	R1, V2ADDR	load v2 source
0000264E	E761 0000 0806		00000000	1831+	VL	v22, 0(R1)	use v21 to test decoder
00002654	E310 5028 0014		00000028	1832+	LGF	R1, V3ADDR	load v3 source
0000265A	E771 0000 0806		00000000	1833+	VL	v23, 0(R1)	use v22 to test decoder
00002660	E756 7030 2E81			1834+	VFENE	V21, V22, V23, 2, 3	test instruction
00002666	B98D 0020			1835+	EPSW	R2, R0	extract psw
0000266A	5020 500C		0000000C	1836+	ST	R2, CCPSW	to save CC
0000266E	E750 5040 080E		00002630	1837+	VST	V21, V1030	save v1 output
00002674	07FB			1838+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002678				1839+RE30	DC	0F	V1 for this test
00002678				1840+	DROP	R5	
00002678	00000000 00000004			1841	DC	XL16' 00000000000000004000000000000000'	V1
00002680	00000000 00000000						
00002688	5D3A5859 25252525			1842	DC	XL16' 5D3A585925252525000000005F444546'	v2
00002690	00000000 5F444546						
00002698	5D3A5859 5A535953			1843	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
000026A0	54454D44 5F444546						
				1844			
				1845 * Word, Not Equal after zero			cc=1
				1846	VRR_B	VFENE, 2, 3, 1	
000026A8				1847+	DS	0FD	
000026A8		000026A8		1848+	USING	*, R5	base for test data and test routine
000026A8	00002700			1849+T31	DC	A(X31)	address of test routine
000026AC	001F			1850+	DC	H' 31'	test number
000026AE	00			1851+	DC	X' 00'	
000026AF	02			1852+	DC	HL1' 2'	m4 used
000026B0	03			1853+	DC	HL1' 3'	m5 used
000026B1	01			1854+	DC	HL1' 1'	CC
000026B2	0B			1855+	DC	HL1' 11'	CC failed mask
000026B4	00000000 00000000			1856+	DS	2F	extracted PSW after test (has CC)
000026BC	FF			1857+	DC	X' FF'	extracted CC, if test failed
000026BD	E5C6C5D5 C5404040			1858+	DC	CL8' VFENE'	instruction name
000026C8	00002730			1859+	DC	A(RE31)	address of v1 result
000026CC	00002740			1860+	DC	A(RE31+16)	address of v2 source
000026D0	00002750			1861+	DC	A(RE31+32)	address of v3 source
000026D4	00000010			1862+	DC	A(16)	result length
000026D8	00002730			1863+REA31	DC	A(RE31)	result address
000026E0	00000000 00000000			1864+	DS	FD	gap
000026E8	00000000 00000000			1865+V1031	DS	XL16	V1 output
000026F0	00000000 00000000						
000026F8	00000000 00000000			1866+	DS	FD	gap
				1867+*			
00002700				1868+X31	DS	0F	
00002700	E310 5024 0014		00000024	1869+	LGF	R1, V2ADDR	load v2 source
00002706	E761 0000 0806		00000000	1870+	VL	v22, 0(R1)	use v21 to test decoder
0000270C	E310 5028 0014		00000028	1871+	LGF	R1, V3ADDR	load v3 source
00002712	E771 0000 0806		00000000	1872+	VL	v23, 0(R1)	use v22 to test decoder
00002718	E756 7030 2E81			1873+	VFENE	V21, V22, V23, 2, 3	test instruction
0000271E	B98D 0020			1874+	EPSW	R2, R0	extract psw
00002722	5020 500C		0000000C	1875+	ST	R2, CCPSW	to save CC
00002726	E750 5040 080E		000026E8	1876+	VST	V21, V1031	save v1 output
0000272C	07FB			1877+	BR	R11	return
00002730				1878+RE31	DC	0F	V1 for this test
00002730				1879+	DROP	R5	
00002730	00000000 00000004			1880	DC	XL16' 00000000000000004000000000000000'	V1
00002738	00000000 00000000						
00002740	5D3A5859 00000000			1881	DC	XL16' 5D3A5859000000000252525255F444546'	v2
00002748	25252525 5F444546						
00002750	5D3A5859 5A535953			1882	DC	XL16' 5D3A58595A53595354454D445F444546'	v3
00002758	54454D44 5F444546						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1884 *	-----	
				1885 *	VFAE - Vector Find Any Element Equal	
				1886 *	-----	
				1887		
				1888 *	-----	
				1889 *	case 0 - simple debug	CC=1 IN=0, RT=0, ZS=0, CS=1
				1890 *	-----	
				1891 *		
				1892	VRR_B VFAE, 0, 1, 1	
00002760				1893+	DS OFD	
00002760		00002760		1894+	USING *, R5	base for test data and test routine
00002760	000027B8			1895+T32	DC A(X32)	address of test routine
00002764	0020			1896+	DC H' 32'	test number
00002766	00			1897+	DC X' 00'	
00002767	00			1898+	DC HL1' 0'	m4 used
00002768	01			1899+	DC HL1' 1'	m5 used
00002769	01			1900+	DC HL1' 1'	CC
0000276A	0B			1901+	DC HL1' 11'	CC failed mask
0000276C	00000000 00000000			1902+	DS 2F	extracted PSW after test (has CC)
00002774	FF			1903+	DC X' FF'	extracted CC, if test failed
00002775	E5C6C1C5 40404040			1904+	DC CL8' VFAE'	instruction name
00002780	000027E8			1905+	DC A(RE32)	address of v1 result
00002784	000027F8			1906+	DC A(RE32+16)	address of v2 source
00002788	00002808			1907+	DC A(RE32+32)	address of v3 source
0000278C	00000010			1908+	DC A(16)	result length
00002790	000027E8			1909+REA32	DC A(RE32)	result address
00002798	00000000 00000000			1910+	DS FD	gap
000027A0	00000000 00000000			1911+V1032	DS XL16	V1 output
000027A8	00000000 00000000					
000027B0	00000000 00000000			1912+	DS FD	gap
				1913+*		
000027B8				1914+X32	DS OF	
000027B8	E310 5024 0014		00000024	1915+	LGF R1, V2ADDR	load v2 source
000027BE	E761 0000 0806		00000000	1916+	VL v22, 0(R1)	use v21 to test decoder
000027C4	E310 5028 0014		00000028	1917+	LGF R1, V3ADDR	load v3 source
000027CA	E771 0000 0806		00000000	1918+	VL v23, 0(R1)	use v22 to test decoder
000027D0	E756 7010 0E82			1919+	VFAE V21, V22, V23, 0, 1	test instruction
000027D6	B98D 0020			1920+	EPSW R2, R0	extract psw
000027DA	5020 500C		0000000C	1921+	ST R2, CCPSW	to save CC
000027DE	E750 5040 080E		000027A0	1922+	VST V21, V1032	save v1 output
000027E4	07FB			1923+	BR R11	return
000027E8				1924+RE32	DC OF	V1 for this test
000027E8				1925+	DROP R5	
000027E8	00000000 00000000			1926	DC XL16' 00000000000000000000000000000000'	V1
000027F0	00000000 00000000					
000027F8	00000000 00000000			1927	DC XL16' 00000000000000000000000000000000'	v2
00002800	00000000 00000000					
00002808	00000000 00000000			1928	DC XL16' 00000000000000000000000000000000'	v3
00002810	00000000 00000000					
				1929		
				1930 *	-----	
				1931 *	case 1 - Hardware Verified	
				1932 *	-----	
				1933 *	Byte, No equal, no zero	
				1934	VRR_B VFAE, 0, 3, 3	cc=3 M5=2+1 ZS CS
00002818				1935+	DS OFD	





LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000028F8	00002978			1988+	DC	A(RE34+32)	address of v3 source
000028FC	00000010			1989+	DC	A(16)	result length
00002900	00002958			1990+REA34	DC	A(RE34)	result address
00002908	00000000 00000000			1991+	DS	FD	gap
00002910	00000000 00000000			1992+V1034	DS	XL16	V1 output
00002918	00000000 00000000						
00002920	00000000 00000000			1993+	DS	FD	gap
				1994+*			
00002928				1995+X34	DS	OF	
00002928	E310 5024 0014		00000024	1996+	LGF	R1, V2ADDR	load v2 source
0000292E	E761 0000 0806		00000000	1997+	VL	v22, 0(R1)	use v21 to test decoder
00002934	E310 5028 0014		00000028	1998+	LGF	R1, V3ADDR	load v3 source
0000293A	E771 0000 0806		00000000	1999+	VL	v23, 0(R1)	use v22 to test decoder
00002940	E756 7070 0E82			2000+	VFAE	V21, V22, V23, 0, 7	test instruction
00002946	B98D 0020			2001+	EPSW	R2, R0	extract psw
0000294A	5020 500C		0000000C	2002+	ST	R2, CCPSW	to save CC
0000294E	E750 5040 080E		00002910	2003+	VST	V21, V1034	save v1 output
00002954	07FB			2004+	BR	R11	return
00002958				2005+RE34	DC	OF	V1 for this test
00002958				2006+	DROP	R5	
00002958	00000000 00000000			2007	DC	XL16' 00000000000000000000000000000000'	V1
00002960	00000000 00000000						
00002968	5D3A5859 5A535953			2008	DC	XL16' 5D3A58595A53595354454D445F444546'	v2
00002970	54454D44 5F444546						
00002978	25252525 25252525			2009	DC	XL16' 25252525252525252525252525252525'	v3
00002980	25252525 25252525						
				2010			
				2011 * Byte, No equal, no zero			
				2012	VRR_B	VFAE, 0, 15, 1	cc=1 M5=8+4+2+1 IN RT ZS CS
00002988				2013+	DS	OFD	
00002988		00002988		2014+	USING	*, R5	base for test data and test routine
00002988	000029E0			2015+T35	DC	A(X35)	address of test routine
0000298C	0023			2016+	DC	H' 35'	test number
0000298E	00			2017+	DC	X' 00'	
0000298F	00			2018+	DC	HL1' 0'	m4 used
00002990	0F			2019+	DC	HL1' 15'	m5 used
00002991	01			2020+	DC	HL1' 1'	CC
00002992	0B			2021+	DC	HL1' 11'	CC failed mask
00002994	00000000 00000000			2022+	DS	2F	extracted PSW after test (has CC)
0000299C	FF			2023+	DC	X' FF'	extracted CC, if test failed
0000299D	E5C6C1C5 40404040			2024+	DC	CL8' VFAE'	instruction name
000029A8	00002A10			2025+	DC	A(RE35)	address of v1 result
000029AC	00002A20			2026+	DC	A(RE35+16)	address of v2 source
000029B0	00002A30			2027+	DC	A(RE35+32)	address of v3 source
000029B4	00000010			2028+	DC	A(16)	result length
000029B8	00002A10			2029+REA35	DC	A(RE35)	result address
000029C0	00000000 00000000			2030+	DS	FD	gap
000029C8	00000000 00000000			2031+V1035	DS	XL16	V1 output
000029D0	00000000 00000000						
000029D8	00000000 00000000			2032+	DS	FD	gap
				2033+*			
000029E0				2034+X35	DS	OF	
000029E0	E310 5024 0014		00000024	2035+	LGF	R1, V2ADDR	load v2 source
000029E6	E761 0000 0806		00000000	2036+	VL	v22, 0(R1)	use v21 to test decoder
000029EC	E310 5028 0014		00000028	2037+	LGF	R1, V3ADDR	load v3 source
000029F2	E771 0000 0806		00000000	2038+	VL	v23, 0(R1)	use v22 to test decoder



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000029F8	E756 70F0 0E82			2039+	VFAE	V21, V22, V23, 0, 15	test instruction	
000029FE	B98D 0020			2040+	EPSW	R2, R0	extract psw	
00002A02	5020 500C		0000000C	2041+	ST	R2, CCPSW	to save CC	
00002A06	E750 5040 080E		000029C8	2042+	VST	V21, V1035	save v1 output	
00002A0C	07FB			2043+	BR	R11	return	
00002A10				2044+RE35	DC	0F	V1 for this test	
00002A10				2045+	DROP	R5		
00002A10	FFFFFFFF FFFFFFFF			2046	DC	XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	V1	
00002A18	FFFFFFFF FFFFFFFF							
00002A20	5D3A5859 5A535953			2047	DC	XL16' 5D3A58595A53595354454D445F444546'	v2	
00002A28	54454D44 5F444546							
00002A30	25252525 25252525			2048	DC	XL16' 25252525252525252525252525252525'	v3	
00002A38	25252525 25252525							
				2049				
				2050 * Byte, No equal, no zero				
				2051	VRR_B	VFAE, 0, 5, 3	cc=3 M5=4+1	RT CS
00002A40				2052+	DS	0FD		
00002A40		00002A40		2053+	USING	*, R5	base for test data and test routine	
00002A40	00002A98			2054+T36	DC	A(X36)	address of test routine	
00002A44	0024			2055+	DC	H' 36'	test number	
00002A46	00			2056+	DC	X' 00'		
00002A47	00			2057+	DC	HL1' 0'	m4 used	
00002A48	05			2058+	DC	HL1' 5'	m5 used	
00002A49	03			2059+	DC	HL1' 3'	CC	
00002A4A	0E			2060+	DC	HL1' 14'	CC failed mask	
00002A4C	00000000 00000000			2061+	DS	2F	extracted PSW after test (has CC)	
00002A54	FF			2062+	DC	X' FF'	extracted CC, if test failed	
00002A55	E5C6C1C5 40404040			2063+	DC	CL8' VFAE'	instruction name	
00002A60	00002AC8			2064+	DC	A(RE36)	address of v1 result	
00002A64	00002AD8			2065+	DC	A(RE36+16)	address of v2 source	
00002A68	00002AE8			2066+	DC	A(RE36+32)	address of v3 source	
00002A6C	00000010			2067+	DC	A(16)	result length	
00002A70	00002AC8			2068+REA36	DC	A(RE36)	result address	
00002A78	00000000 00000000			2069+	DS	FD	gap	
00002A80	00000000 00000000			2070+V1036	DS	XL16	V1 output	
00002A88	00000000 00000000							
00002A90	00000000 00000000			2071+	DS	FD	gap	
				2072+*				
00002A98				2073+X36	DS	0F		
00002A98	E310 5024 0014		00000024	2074+	LGF	R1, V2ADDR	load v2 source	
00002A9E	E761 0000 0806		00000000	2075+	VL	v22, 0(R1)	use v21 to test decoder	
00002AA4	E310 5028 0014		00000028	2076+	LGF	R1, V3ADDR	load v3 source	
00002AAA	E771 0000 0806		00000000	2077+	VL	v23, 0(R1)	use v22 to test decoder	
00002AB0	E756 7050 0E82			2078+	VFAE	V21, V22, V23, 0, 5	test instruction	
00002AB6	B98D 0020			2079+	EPSW	R2, R0	extract psw	
00002ABA	5020 500C		0000000C	2080+	ST	R2, CCPSW	to save CC	
00002ABE	E750 5040 080E		00002A80	2081+	VST	V21, V1036	save v1 output	
00002AC4	07FB			2082+	BR	R11	return	
00002AC8				2083+RE36	DC	0F	V1 for this test	
00002AC8				2084+	DROP	R5		
00002AC8	00000000 00000000			2085	DC	XL16' 00000000000000000000000000000000'	V1	
00002AD0	00000000 00000000							
00002AD8	5D3A5859 5A535953			2086	DC	XL16' 5D3A58595A53595354454D445F444546'	v2	
00002AE0	54454D44 5F444546							
00002AE8	25252525 25252525			2087	DC	XL16' 25252525252525252525252525252525'	v3	
00002AF0	25252525 25252525							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2088		
				2089 * Byte, No equal, no zero		
				2090	VRR_B VFAE, 0, 13, 1	cc=1 M5=8=4+1    IN RT    CS
00002AF8				2091+	DS    OFD	
00002AF8		00002AF8		2092+	USING *, R5	base for test data and test routine
00002AF8	00002B50			2093+T37	DC    A(X37)	address of test routine
00002AFC	0025			2094+	DC    H' 37'	test number
00002AFE	00			2095+	DC    X' 00'	
00002AFF	00			2096+	DC    HL1' 0'	m4 used
00002B00	0D			2097+	DC    HL1' 13'	m5 used
00002B01	01			2098+	DC    HL1' 1'	CC
00002B02	0B			2099+	DC    HL1' 11'	CC failed mask
00002B04	00000000 00000000			2100+	DS    2F	extracted PSW after test (has CC)
00002B0C	FF			2101+	DC    X' FF'	extracted CC, if test failed
00002B0D	E5C6C1C5 40404040			2102+	DC    CL8' VFAE'	instruction name
00002B18	00002B80			2103+	DC    A(RE37)	address of v1 result
00002B1C	00002B90			2104+	DC    A(RE37+16)	address of v2 source
00002B20	00002BA0			2105+	DC    A(RE37+32)	address of v3 source
00002B24	00000010			2106+	DC    A(16)	result length
00002B28	00002B80			2107+REA37	DC    A(RE37)	result address
00002B30	00000000 00000000			2108+	DS    FD	gap
00002B38	00000000 00000000			2109+V1037	DS    XL16	V1 output
00002B40	00000000 00000000					
00002B48	00000000 00000000			2110+	DS    FD	gap
				2111+*		
00002B50				2112+X37	DS    0F	
00002B50	E310 5024 0014		00000024	2113+	LGF    R1, V2ADDR	load v2 source
00002B56	E761 0000 0806		00000000	2114+	VL    v22, 0(R1)	use v21 to test decoder
00002B5C	E310 5028 0014		00000028	2115+	LGF    R1, V3ADDR	load v3 source
00002B62	E771 0000 0806		00000000	2116+	VL    v23, 0(R1)	use v22 to test decoder
00002B68	E756 70D0 0E82			2117+	VFAE    V21, V22, V23, 0, 13	test instruction
00002B6E	B98D 0020			2118+	EPSW    R2, R0	extract psw
00002B72	5020 500C		0000000C	2119+	ST    R2, CCPSW	to save CC
00002B76	E750 5040 080E		00002B38	2120+	VST    V21, V1037	save v1 output
00002B7C	07FB			2121+	BR    R11	return
00002B80				2122+RE37	DC    0F	V1 for this test
00002B80				2123+	DROP    R5	
00002B80	FFFFFFFF FFFFFFFF			2124	DC    XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	V1
00002B88	FFFFFFFF FFFFFFFF					
00002B90	5D3A5859 5A535953			2125	DC    XL16' 5D3A58595A53595354454D445F444546'	v2
00002B98	54454D44 5F444546					
00002BA0	25252525 25252525			2126	DC    XL16' 25252525252525252525252525252525'	v3
00002BA8	25252525 25252525					

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2128 *	-----		
				2129 *	Byte, Equal, no zero		
00002BB0				2130	VRR_B VFAE, 0, 3, 1	cc=1 M5=2+1	ZS CS
00002BB0		00002BB0		2131+	DS OFD		
00002BB0	00002C08			2132+	USING *, R5	base for test data and test routine	
00002BB4	0026			2133+T38	DC A(X38)	address of test routine	
00002BB6	00			2134+	DC H' 38'	test number	
00002BB7	00			2135+	DC X' 00'		
00002BB8	03			2136+	DC HL1' 0'	m4 used	
00002BB9	01			2137+	DC HL1' 3'	m5 used	
00002BBA	0B			2138+	DC HL1' 1'	CC	
00002BBC	00000000 00000000			2139+	DC HL1' 11'	CC failed mask	
00002BC4	FF			2140+	DS 2F	extracted PSW after test (has CC)	
00002BC5	E5C6C1C5 40404040			2141+	DC X' FF'	extracted CC, if test failed	
00002BD0	00002C38			2142+	DC CL8' VFAE'	instruction name	
00002BD4	00002C48			2143+	DC A(RE38)	address of v1 result	
00002BD8	00002C58			2144+	DC A(RE38+16)	address of v2 source	
00002BDC	00000010			2145+	DC A(RE38+32)	address of v3 source	
00002BE0	00002C38			2146+	DC A(16)	result length	
00002BE8	00000000 00000000			2147+REA38	DC A(RE38)	result address	
00002BF0	00000000 00000000			2148+	DS FD	gap	
00002BF8	00000000 00000000			2149+V1038	DS XL16	V1 output	
00002C00	00000000 00000000			2150+	DS FD	gap	
				2151+*			
00002C08				2152+X38	DS OF		
00002C08	E310 5024 0014		00000024	2153+	LGF R1, V2ADDR	load v2 source	
00002C0E	E761 0000 0806		00000000	2154+	VL v22, 0(R1)	use v21 to test decoder	
00002C14	E310 5028 0014		00000028	2155+	LGF R1, V3ADDR	load v3 source	
00002C1A	E771 0000 0806		00000000	2156+	VL v23, 0(R1)	use v22 to test decoder	
00002C20	E756 7030 0E82			2157+	VFAE V21, V22, V23, 0, 3	test instruction	
00002C26	B98D 0020			2158+	EPSW R2, R0	extract psw	
00002C2A	5020 500C		0000000C	2159+	ST R2, CCPSW	to save CC	
00002C2E	E750 5040 080E		00002BF0	2160+	VST V21, V1038	save v1 output	
00002C34	07FB			2161+	BR R11	return	
00002C38				2162+RE38	DC OF	V1 for this test	
00002C38				2163+	DROP R5		
00002C38	00000000 00000005			2164	DC XL16' 00000000000000005000000000000000'	V1	
00002C40	00000000 00000000						
00002C48	5D3A5859 5A255953			2165	DC XL16' 5D3A58595A25595354454D445F444546'	v2	
00002C50	54454D44 5F444546						
00002C58	25252525 25252525			2166	DC XL16' 25252525252525252525252525252525'	v3	
00002C60	25252525 25252525						
				2167			
				2168 *	Byte, Equal, no zero		
				2169	VRR_B VFAE, 0, 7, 1	cc=1 M5=4+2+1	RT ZS CS
00002C68				2170+	DS OFD		
00002C68		00002C68		2171+	USING *, R5	base for test data and test routine	
00002C68	00002CC0			2172+T39	DC A(X39)	address of test routine	
00002C6C	0027			2173+	DC H' 39'	test number	
00002C6E	00			2174+	DC X' 00'		
00002C6F	00			2175+	DC HL1' 0'	m4 used	
00002C70	07			2176+	DC HL1' 7'	m5 used	
00002C71	01			2177+	DC HL1' 1'	CC	
00002C72	0B			2178+	DC HL1' 11'	CC failed mask	
00002C74	00000000 00000000			2179+	DS 2F	extracted PSW after test (has CC)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002C7C	FF			2180+	DC	X' FF'	extracted CC, if test failed
00002C7D	E5C6C1C5 40404040			2181+	DC	CL8' VFAE'	instruction name
00002C88	00002CF0			2182+	DC	A(RE39)	address of v1 result
00002C8C	00002D00			2183+	DC	A(RE39+16)	address of v2 source
00002C90	00002D10			2184+	DC	A(RE39+32)	address of v3 source
00002C94	00000010			2185+	DC	A(16)	result length
00002C98	00002CF0			2186+REA39	DC	A(RE39)	result address
00002CA0	00000000 00000000			2187+	DS	FD	gap
00002CA8	00000000 00000000			2188+V1039	DS	XL16	V1 output
00002CB0	00000000 00000000						
00002CB8	00000000 00000000			2189+	DS	FD	gap
				2190+*			
00002CC0				2191+X39	DS	0F	
00002CC0	E310 5024 0014		00000024	2192+	LGF	R1, V2ADDR	load v2 source
00002CC6	E761 0000 0806		00000000	2193+	VL	v22, 0(R1)	use v21 to test decoder
00002CCC	E310 5028 0014		00000028	2194+	LGF	R1, V3ADDR	load v3 source
00002CD2	E771 0000 0806		00000000	2195+	VL	v23, 0(R1)	use v22 to test decoder
00002CD8	E756 7070 0E82			2196+	VFAE	V21, V22, V23, 0, 7	test instruction
00002CDE	B98D 0020			2197+	EPSW	R2, R0	extract psw
00002CE2	5020 500C		0000000C	2198+	ST	R2, CCPSW	to save CC
00002CE6	E750 5040 080E		00002CA8	2199+	VST	V21, V1039	save v1 output
00002CEC	07FB			2200+	BR	R11	return
00002CF0				2201+RE39	DC	0F	V1 for this test
00002CF0				2202+	DROP	R5	
00002CF0	00000000 00FF0000			2203	DC	XL16' 0000000000FF000000000000000000000'	V1
00002CF8	00000000 00000000						
00002D00	5D3A5859 5A255953			2204	DC	XL16' 5D3A58595A25595354454D445F444546'	v2
00002D08	54454D44 5F444546						
00002D10	25252525 25252525			2205	DC	XL16' 25252525252525252525252525252525'	v3
00002D18	25252525 25252525						
				2206			
				2207 * Byte, Equal, no zero			
				2208	VRR_B	VFAE, 0, 15, 1	cc=1 M5=8+4+2+1 IN RT ZS CS
00002D20				2209+	DS	0FD	
00002D20		00002D20		2210+	USING	*, R5	base for test data and test routine
00002D20	00002D78			2211+T40	DC	A(X40)	address of test routine
00002D24	0028			2212+	DC	H' 40'	test number
00002D26	00			2213+	DC	X' 00'	
00002D27	00			2214+	DC	HL1' 0'	m4 used
00002D28	0F			2215+	DC	HL1' 15'	m5 used
00002D29	01			2216+	DC	HL1' 1'	CC
00002D2A	0B			2217+	DC	HL1' 11'	CC failed mask
00002D2C	00000000 00000000			2218+	DS	2F	extracted PSW after test (has CC)
00002D34	FF			2219+	DC	X' FF'	extracted CC, if test failed
00002D35	E5C6C1C5 40404040			2220+	DC	CL8' VFAE'	instruction name
00002D40	00002DA8			2221+	DC	A(RE40)	address of v1 result
00002D44	00002DB8			2222+	DC	A(RE40+16)	address of v2 source
00002D48	00002DC8			2223+	DC	A(RE40+32)	address of v3 source
00002D4C	00000010			2224+	DC	A(16)	result length
00002D50	00002DA8			2225+REA40	DC	A(RE40)	result address
00002D58	00000000 00000000			2226+	DS	FD	gap
00002D60	00000000 00000000			2227+V1040	DS	XL16	V1 output
00002D68	00000000 00000000						
00002D70	00000000 00000000			2228+	DS	FD	gap
				2229+*			
00002D78				2230+X40	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002D78	E310 5024 0014		00000024	2231+	LGF	R1, V2ADDR	load v2 source
00002D7E	E761 0000 0806		00000000	2232+	VL	v22, 0(R1)	use v21 to test decoder
00002D84	E310 5028 0014		00000028	2233+	LGF	R1, V3ADDR	load v3 source
00002D8A	E771 0000 0806		00000000	2234+	VL	v23, 0(R1)	use v22 to test decoder
00002D90	E756 70F0 0E82			2235+	VFAE	V21, V22, V23, 0, 15	test instruction
00002D96	B98D 0020			2236+	EPSW	R2, R0	extract psw
00002D9A	5020 500C		0000000C	2237+	ST	R2, CCPSW	to save CC
00002D9E	E750 5040 080E		00002D60	2238+	VST	V21, V1040	save v1 output
00002DA4	07FB			2239+	BR	R11	return
00002DA8				2240+RE40	DC	0F	V1 for this test
00002DA8				2241+	DROP	R5	
00002DA8	FFFFFFFF FF00FFFF			2242	DC	XL16' FFFFFFFFFF00FFFFFFFFFFFFFFFFFFFF'	V1
00002DB0	FFFFFFFF FFFFFFFF						
00002DB8	5D3A5859 5A255953			2243	DC	XL16' 5D3A58595A25595354454D445F444546'	v2
00002DC0	54454D44 5F444546						
00002DC8	25252525 25252525			2244	DC	XL16' 25252525252525252525252525252525'	v3
00002DD0	25252525 25252525						
				2245			
				2246 * Byte, Equal, no zero			
				2247 VRR_B VFAE, 0, 1, 1		cc=1 M5=1	CS
00002DD8				2248+	DS	0FD	
00002DD8		00002DD8		2249+	USING	*, R5	base for test data and test routine
00002DD8	00002E30			2250+T41	DC	A(X41)	address of test routine
00002DDC	0029			2251+	DC	H' 41'	test number
00002DDE	00			2252+	DC	X' 00'	
00002DDF	00			2253+	DC	HL1' 0'	m4 used
00002DE0	01			2254+	DC	HL1' 1'	m5 used
00002DE1	01			2255+	DC	HL1' 1'	CC
00002DE2	0B			2256+	DC	HL1' 11'	CC failed mask
00002DE4	00000000 00000000			2257+	DS	2F	extracted PSW after test (has CC)
00002DEC	FF			2258+	DC	X' FF'	extracted CC, if test failed
00002DED	E5C6C1C5 40404040			2259+	DC	CL8' VFAE'	instruction name
00002DF8	00002E60			2260+	DC	A(RE41)	address of v1 result
00002DFC	00002E70			2261+	DC	A(RE41+16)	address of v2 source
00002E00	00002E80			2262+	DC	A(RE41+32)	address of v3 source
00002E04	00000010			2263+	DC	A(16)	result length
00002E08	00002E60			2264+REA41	DC	A(RE41)	result address
00002E10	00000000 00000000			2265+	DS	FD	gap
00002E18	00000000 00000000			2266+V1041	DS	XL16	V1 output
00002E20	00000000 00000000						
00002E28	00000000 00000000			2267+	DS	FD	gap
				2268+*			
00002E30				2269+X41	DS	0F	
00002E30	E310 5024 0014		00000024	2270+	LGF	R1, V2ADDR	load v2 source
00002E36	E761 0000 0806		00000000	2271+	VL	v22, 0(R1)	use v21 to test decoder
00002E3C	E310 5028 0014		00000028	2272+	LGF	R1, V3ADDR	load v3 source
00002E42	E771 0000 0806		00000000	2273+	VL	v23, 0(R1)	use v22 to test decoder
00002E48	E756 7010 0E82			2274+	VFAE	V21, V22, V23, 0, 1	test instruction
00002E4E	B98D 0020			2275+	EPSW	R2, R0	extract psw
00002E52	5020 500C		0000000C	2276+	ST	R2, CCPSW	to save CC
00002E56	E750 5040 080E		00002E18	2277+	VST	V21, V1041	save v1 output
00002E5C	07FB			2278+	BR	R11	return
00002E60				2279+RE41	DC	0F	V1 for this test
00002E60				2280+	DROP	R5	
00002E60	00000000 00000005			2281	DC	XL16' 00000000000000050000000000000000'	V1
00002E68	00000000 00000000						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002E70	5D3A5859 5A255953			2282	DC	XL16' 5D3A58595A25595354454D445F444546'	v2	
00002E78	54454D44 5F444546							
00002E80	25252525 25252525			2283	DC	XL16' 25252525252525252525252525252525'	v3	
00002E88	25252525 25252525							
				2284				
				2285	* Byte, Equal, no zero			
				2286	VRR_B VFAE, 0, 5, 1	cc=1 M5=4+1	RT	CS
00002E90				2287+	DS	0FD		
00002E90		00002E90		2288+	USING	*, R5	base for test data and test routine	
00002E90	00002EE8			2289+T42	DC	A(X42)	address of test routine	
00002E94	002A			2290+	DC	H' 42'	test number	
00002E96	00			2291+	DC	X' 00'		
00002E97	00			2292+	DC	HL1' 0'	m4 used	
00002E98	05			2293+	DC	HL1' 5'	m5 used	
00002E99	01			2294+	DC	HL1' 1'	CC	
00002E9A	0B			2295+	DC	HL1' 11'	CC failed mask	
00002E9C	00000000 00000000			2296+	DS	2F	extracted PSW after test (has CC)	
00002EA4	FF			2297+	DC	X' FF'	extracted CC, if test failed	
00002EA5	E5C6C1C5 40404040			2298+	DC	CL8' VFAE'	instruction name	
00002EB0	00002F18			2299+	DC	A(RE42)	address of v1 result	
00002EB4	00002F28			2300+	DC	A(RE42+16)	address of v2 source	
00002EB8	00002F38			2301+	DC	A(RE42+32)	address of v3 source	
00002EBC	00000010			2302+	DC	A(16)	result length	
00002EC0	00002F18			2303+REA42	DC	A(RE42)	result address	
00002EC8	00000000 00000000			2304+	DS	FD	gap	
00002ED0	00000000 00000000			2305+V1042	DS	XL16	V1 output	
00002ED8	00000000 00000000							
00002EE0	00000000 00000000			2306+	DS	FD	gap	
				2307+*				
00002EE8				2308+X42	DS	0F		
00002EE8	E310 5024 0014		00000024	2309+	LGF	R1, V2ADDR	load v2 source	
00002EEE	E761 0000 0806		00000000	2310+	VL	v22, 0(R1)	use v21 to test decoder	
00002EF4	E310 5028 0014		00000028	2311+	LGF	R1, V3ADDR	load v3 source	
00002EFA	E771 0000 0806		00000000	2312+	VL	v23, 0(R1)	use v22 to test decoder	
00002F00	E756 7050 0E82			2313+	VFAE	V21, V22, V23, 0, 5	test instruction	
00002F06	B98D 0020			2314+	EPSW	R2, R0	extract psw	
00002F0A	5020 500C		0000000C	2315+	ST	R2, CCPSW	to save CC	
00002F0E	E750 5040 080E		00002ED0	2316+	VST	V21, V1042	save v1 output	
00002F14	07FB			2317+	BR	R11	return	
00002F18				2318+RE42	DC	0F	V1 for this test	
00002F18				2319+	DROP	R5		
00002F18	00000000 00FF0000			2320	DC	XL16' 0000000000FF0000000000000000000'	V1	
00002F20	00000000 00000000							
00002F28	5D3A5859 5A255953			2321	DC	XL16' 5D3A58595A25595354454D445F444546'	v2	
00002F30	54454D44 5F444546							
00002F38	25252525 25252525			2322	DC	XL16' 25252525252525252525252525252525'	v3	
00002F40	25252525 25252525							
				2323				
				2324	* Byte, Equal, no zero			
				2325	VRR_B VFAE, 0, 13, 1	cc=1 M5=8+4+1	IN RT	CS
00002F48				2326+	DS	0FD		
00002F48		00002F48		2327+	USING	*, R5	base for test data and test routine	
00002F48	00002FA0			2328+T43	DC	A(X43)	address of test routine	
00002F4C	002B			2329+	DC	H' 43'	test number	
00002F4E	00			2330+	DC	X' 00'		
00002F4F	00			2331+	DC	HL1' 0'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002F50	0D			2332+	DC	HL1' 13'	m5 used
00002F51	01			2333+	DC	HL1' 1'	CC
00002F52	0B			2334+	DC	HL1' 11'	CC failed mask
00002F54	00000000 00000000			2335+	DS	2F	extracted PSW after test (has CC)
00002F5C	FF			2336+	DC	X' FF'	extracted CC, if test failed
00002F5D	E5C6C1C5 40404040			2337+	DC	CL8' VFAE'	instruction name
00002F68	00002FD0			2338+	DC	A(RE43)	address of v1 result
00002F6C	00002FE0			2339+	DC	A(RE43+16)	address of v2 source
00002F70	00002FF0			2340+	DC	A(RE43+32)	address of v3 source
00002F74	00000010			2341+	DC	A(16)	result length
00002F78	00002FD0			2342+REA43	DC	A(RE43)	result address
00002F80	00000000 00000000			2343+	DS	FD	gap
00002F88	00000000 00000000			2344+V1043	DS	XL16	V1 output
00002F90	00000000 00000000						
00002F98	00000000 00000000			2345+	DS	FD	gap
				2346+*			
00002FA0				2347+X43	DS	0F	
00002FA0	E310 5024 0014		00000024	2348+	LGF	R1, V2ADDR	load v2 source
00002FA6	E761 0000 0806		00000000	2349+	VL	v22, 0(R1)	use v21 to test decoder
00002FAC	E310 5028 0014		00000028	2350+	LGF	R1, V3ADDR	load v3 source
00002FB2	E771 0000 0806		00000000	2351+	VL	v23, 0(R1)	use v22 to test decoder
00002FB8	E756 70D0 0E82			2352+	VFAE	V21, V22, V23, 0, 13	test instruction
00002FBE	B98D 0020			2353+	EPSW	R2, R0	extract psw
00002FC2	5020 500C		0000000C	2354+	ST	R2, CCPSW	to save CC
00002FC6	E750 5040 080E		00002F88	2355+	VST	V21, V1043	save v1 output
00002FCC	07FB			2356+	BR	R11	return
00002FD0				2357+RE43	DC	0F	V1 for this test
00002FD0				2358+	DROP	R5	
00002FD0	FFFFFFFF FF00FFFF			2359	DC	XL16' FFFFFFFFFF00FFFFFFFFFFFFFFFFFFFFFF'	V1
00002FD8	FFFFFFFF FFFFFFFF						
00002FE0	5D3A5859 5A255953			2360	DC	XL16' 5D3A58595A25595354454D445F444546'	v2
00002FE8	54454D44 5F444546						
00002FF0	25252525 25252525			2361	DC	XL16' 25252525252525252525252525252525'	v3
00002FF8	25252525 25252525						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2363 *-----	
				2364 * Byte, Equal before zero	
00003000				2365 VRR_B VFAE, 0, 3, 2	cc=2 M5=2+1 ZS CS
00003000		00003000		2366+ DS OFD	
00003000	00003058			2367+ USING *, R5	base for test data and test routine
00003004	002C			2368+T44 DC A(X44)	address of test routine
00003006	00			2369+ DC H' 44'	test number
00003007	00			2370+ DC X' 00'	
00003008	03			2371+ DC HL1' 0'	m4 used
00003009	02			2372+ DC HL1' 3'	m5 used
0000300A	0D			2373+ DC HL1' 2'	CC
0000300C	00000000 00000000			2374+ DC HL1' 13'	CC failed mask
00003014	FF			2375+ DS 2F	extracted PSW after test (has CC)
00003015	E5C6C1C5 40404040			2376+ DC X' FF'	extracted CC, if test failed
00003020	00003088			2377+ DC CL8' VFAE'	instruction name
00003024	00003098			2378+ DC A(RE44)	address of v1 result
00003028	000030A8			2379+ DC A(RE44+16)	address of v2 source
0000302C	00000010			2380+ DC A(RE44+32)	address of v3 source
00003030	00003088			2381+ DC A(16)	result length
00003038	00000000 00000000			2382+REA44 DC A(RE44)	result address
00003040	00000000 00000000			2383+ DS FD	gap
00003048	00000000 00000000			2384+V1044 DS XL16	V1 output
00003050	00000000 00000000			2385+ DS FD	gap
				2386+*	
00003058				2387+X44 DS OF	
00003058	E310 5024 0014	00000024		2388+ LGF R1, V2ADDR	load v2 source
0000305E	E761 0000 0806	00000000		2389+ VL v22, 0(R1)	use v21 to test decoder
00003064	E310 5028 0014	00000028		2390+ LGF R1, V3ADDR	load v3 source
0000306A	E771 0000 0806	00000000		2391+ VL v23, 0(R1)	use v22 to test decoder
00003070	E756 7030 0E82			2392+ VFAE V21, V22, V23, 0, 3	test instruction
00003076	B98D 0020			2393+ EPSW R2, R0	extract psw
0000307A	5020 500C	0000000C		2394+ ST R2, CCPSW	to save CC
0000307E	E750 5040 080E	00003040		2395+ VST V21, V1044	save v1 output
00003084	07FB			2396+ BR R11	return
00003088				2397+RE44 DC OF	V1 for this test
00003088				2398+ DROP R5	
00003088	00000000 00000005			2399 DC XL16' 00000000 00000005 00000000 00000000'	V1
00003090	00000000 00000000				
00003098	5D3A5859 5A255953		2400	DC XL16' 5D3A5859 5A255953 54004D44 5F444546'	v2
000030A0	54004D44 5F444546				
000030A8	25252525 25252525		2401	DC XL16' 25252525 25252525 25252525 25252525'	v3
000030B0	25252525 25252525				
				2402	
				2403 * Byte, Equal before zero	
000030B8				2404 VRR_B VFAE, 0, 7, 2	cc=2 M5=4+2+1 RT ZS CS
000030B8		000030B8		2405+ DS OFD	
000030B8	00003110			2406+ USING *, R5	base for test data and test routine
000030BC	002D			2407+T45 DC A(X45)	address of test routine
000030BE	00			2408+ DC H' 45'	test number
000030BF	00			2409+ DC X' 00'	
000030C0	07			2410+ DC HL1' 0'	m4 used
000030C1	02			2411+ DC HL1' 7'	m5 used
000030C2	0D			2412+ DC HL1' 2'	CC
000030C4	00000000 00000000			2413+ DC HL1' 13'	CC failed mask
				2414+ DS 2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000030CC	FF			2415+	DC	X' FF'	extracted CC, if test failed		
000030CD	E5C6C1C5 40404040			2416+	DC	CL8' VFAE'	instruction name		
000030D8	00003140			2417+	DC	A(RE45)	address of v1 result		
000030DC	00003150			2418+	DC	A(RE45+16)	address of v2 source		
000030E0	00003160			2419+	DC	A(RE45+32)	address of v3 source		
000030E4	00000010			2420+	DC	A(16)	result length		
000030E8	00003140			2421+REA45	DC	A(RE45)	result address		
000030F0	00000000 00000000			2422+	DS	FD	gap		
000030F8	00000000 00000000			2423+V1045	DS	XL16	V1 output		
00003100	00000000 00000000								
00003108	00000000 00000000			2424+	DS	FD	gap		
				2425+*					
00003110				2426+X45	DS	0F			
00003110	E310 5024 0014		00000024	2427+	LGF	R1, V2ADDR	load v2 source		
00003116	E761 0000 0806		00000000	2428+	VL	v22, 0(R1)	use v21 to test decoder		
0000311C	E310 5028 0014		00000028	2429+	LGF	R1, V3ADDR	load v3 source		
00003122	E771 0000 0806		00000000	2430+	VL	v23, 0(R1)	use v22 to test decoder		
00003128	E756 7070 0E82			2431+	VFAE	V21, V22, V23, 0, 7	test instruction		
0000312E	B98D 0020			2432+	EPSW	R2, R0	extract psw		
00003132	5020 500C		0000000C	2433+	ST	R2, CCPSW	to save CC		
00003136	E750 5040 080E		000030F8	2434+	VST	V21, V1045	save v1 output		
0000313C	07FB			2435+	BR	R11	return		
00003140				2436+RE45	DC	0F	V1 for this test		
00003140				2437+	DROP	R5			
00003140	00000000 00FF0000			2438	DC	XL16' 00000000 00FF0000 00000000 00000000'	V1		
00003148	00000000 00000000								
00003150	5D3A5859 5A255953			2439	DC	XL16' 5D3A5859 5A255953 54004D44 5F444546'	v2		
00003158	54004D44 5F444546								
00003160	25252525 25252525			2440	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003168	25252525 25252525								
				2441					
				2442 * Byte, Equal before zero					
				2443	VRR_B	VFAE, 0, 15, 2	cc=2 M5=8+4+2+1 IN RT ZS CS		
00003170				2444+	DS	0FD			
00003170		00003170		2445+	USING	*, R5	base for test data and test routine		
00003170	000031C8			2446+T46	DC	A(X46)	address of test routine		
00003174	002E			2447+	DC	H' 46'	test number		
00003176	00			2448+	DC	X' 00'			
00003177	00			2449+	DC	HL1' 0'	m4 used		
00003178	0F			2450+	DC	HL1' 15'	m5 used		
00003179	02			2451+	DC	HL1' 2'	CC		
0000317A	0D			2452+	DC	HL1' 13'	CC failed mask		
0000317C	00000000 00000000			2453+	DS	2F	extracted PSW after test (has CC)		
00003184	FF			2454+	DC	X' FF'	extracted CC, if test failed		
00003185	E5C6C1C5 40404040			2455+	DC	CL8' VFAE'	instruction name		
00003190	000031F8			2456+	DC	A(RE46)	address of v1 result		
00003194	00003208			2457+	DC	A(RE46+16)	address of v2 source		
00003198	00003218			2458+	DC	A(RE46+32)	address of v3 source		
0000319C	00000010			2459+	DC	A(16)	result length		
000031A0	000031F8			2460+REA46	DC	A(RE46)	result address		
000031A8	00000000 00000000			2461+	DS	FD	gap		
000031B0	00000000 00000000			2462+V1046	DS	XL16	V1 output		
000031B8	00000000 00000000								
000031C0	00000000 00000000			2463+	DS	FD	gap		
				2464+*					
000031C8				2465+X46	DS	0F			



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000031C8	E310 5024 0014		00000024	2466+	LGF	R1, V2ADDR	load v2 source		
000031CE	E761 0000 0806		00000000	2467+	VL	v22, 0(R1)	use v21 to test decoder		
000031D4	E310 5028 0014		00000028	2468+	LGF	R1, V3ADDR	load v3 source		
000031DA	E771 0000 0806		00000000	2469+	VL	v23, 0(R1)	use v22 to test decoder		
000031E0	E756 70F0 0E82			2470+	VFAE	V21, V22, V23, 0, 15	test instruction		
000031E6	B98D 0020			2471+	EPSW	R2, R0	extract psw		
000031EA	5020 500C		0000000C	2472+	ST	R2, CCPSW	to save CC		
000031EE	E750 5040 080E		000031B0	2473+	VST	V21, V1046	save v1 output		
000031F4	07FB			2474+	BR	R11	return		
000031F8				2475+RE46	DC	0F	V1 for this test		
000031F8				2476+	DROP	R5			
000031F8	FFFFFFFF FF00FFFF			2477	DC	XL16' FFFFFFFFFF FF00FFFF FFFFFFFFFF FFFFFFFFFF'	V1		
00003200	FFFFFFFF FFFFFFFFFF								
00003208	5D3A5859 5A255953			2478	DC	XL16' 5D3A5859 5A255953 54004D44 5F444546'	v2		
00003210	54004D44 5F444546								
00003218	25252525 25252525			2479	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003220	25252525 25252525								
				2480					
				2481 * Byte, Equal before zero					
				2482	VRR_B	VFAE, 0, 1, 1	cc=1 M5=1		CS
00003228				2483+	DS	0FD			
00003228		00003228		2484+	USING	*, R5	base for test data and test routine		
00003228	00003280			2485+T47	DC	A(X47)	address of test routine		
0000322C	002F			2486+	DC	H' 47'	test number		
0000322E	00			2487+	DC	X' 00'			
0000322F	00			2488+	DC	HL1' 0'	m4 used		
00003230	01			2489+	DC	HL1' 1'	m5 used		
00003231	01			2490+	DC	HL1' 1'	CC		
00003232	0B			2491+	DC	HL1' 11'	CC failed mask		
00003234	00000000 00000000			2492+	DS	2F	extracted PSW after test (has CC)		
0000323C	FF			2493+	DC	X' FF'	extracted CC, if test failed		
0000323D	E5C6C1C5 40404040			2494+	DC	CL8' VFAE'	instruction name		
00003248	000032B0			2495+	DC	A(RE47)	address of v1 result		
0000324C	000032C0			2496+	DC	A(RE47+16)	address of v2 source		
00003250	000032D0			2497+	DC	A(RE47+32)	address of v3 source		
00003254	00000010			2498+	DC	A(16)	result length		
00003258	000032B0			2499+REA47	DC	A(RE47)	result address		
00003260	00000000 00000000			2500+	DS	FD	gap		
00003268	00000000 00000000			2501+V1047	DS	XL16	V1 output		
00003270	00000000 00000000								
00003278	00000000 00000000			2502+	DS	FD	gap		
				2503+*					
00003280				2504+X47	DS	0F			
00003280	E310 5024 0014		00000024	2505+	LGF	R1, V2ADDR	load v2 source		
00003286	E761 0000 0806		00000000	2506+	VL	v22, 0(R1)	use v21 to test decoder		
0000328C	E310 5028 0014		00000028	2507+	LGF	R1, V3ADDR	load v3 source		
00003292	E771 0000 0806		00000000	2508+	VL	v23, 0(R1)	use v22 to test decoder		
00003298	E756 7010 0E82			2509+	VFAE	V21, V22, V23, 0, 1	test instruction		
0000329E	B98D 0020			2510+	EPSW	R2, R0	extract psw		
000032A2	5020 500C		0000000C	2511+	ST	R2, CCPSW	to save CC		
000032A6	E750 5040 080E		00003268	2512+	VST	V21, V1047	save v1 output		
000032AC	07FB			2513+	BR	R11	return		
000032B0				2514+RE47	DC	0F	V1 for this test		
000032B0				2515+	DROP	R5			
000032B0	00000000 00000005			2516	DC	XL16' 00000000 00000005 00000000 00000000'	V1		
000032B8	00000000 00000000								



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
000032C0	5D3A5859 5A255953			2517	DC	XL16'	5D3A5859 5A255953 54004D44 5F444546'	v2		
000032C8	54004D44 5F444546									
000032D0	25252525 25252525			2518	DC	XL16'	25252525 25252525 25252525 25252525'	v3		
000032D8	25252525 25252525									
				2519						
				2520	* Byte, Equal before zero					
				2521	VRR_B	VFAE, 0, 5, 1		cc=1 M5=4+1	RT	CS
000032E0				2522+	DS	0FD				
000032E0		000032E0		2523+	USING	*, R5		base for test data and test routine		
000032E0	00003338			2524+T48	DC	A(X48)		address of test routine		
000032E4	0030			2525+	DC	H' 48'		test number		
000032E6	00			2526+	DC	X' 00'				
000032E7	00			2527+	DC	HL1' 0'		m4 used		
000032E8	05			2528+	DC	HL1' 5'		m5 used		
000032E9	01			2529+	DC	HL1' 1'		CC		
000032EA	0B			2530+	DC	HL1' 11'		CC failed mask		
000032EC	00000000 00000000			2531+	DS	2F		extracted PSW after test (has CC)		
000032F4	FF			2532+	DC	X' FF'		extracted CC, if test failed		
000032F5	E5C6C1C5 40404040			2533+	DC	CL8' VFAE'		instruction name		
00003300	00003368			2534+	DC	A(RE48)		address of v1 result		
00003304	00003378			2535+	DC	A(RE48+16)		address of v2 source		
00003308	00003388			2536+	DC	A(RE48+32)		address of v3 source		
0000330C	00000010			2537+	DC	A(16)		result length		
00003310	00003368			2538+REA48	DC	A(RE48)		result address		
00003318	00000000 00000000			2539+	DS	FD		gap		
00003320	00000000 00000000			2540+V1048	DS	XL16		V1 output		
00003328	00000000 00000000									
00003330	00000000 00000000			2541+	DS	FD		gap		
				2542+*						
00003338				2543+X48	DS	0F				
00003338	E310 5024 0014		00000024	2544+	LGF	R1, V2ADDR		load v2 source		
0000333E	E761 0000 0806		00000000	2545+	VL	v22, 0(R1)		use v21 to test decoder		
00003344	E310 5028 0014		00000028	2546+	LGF	R1, V3ADDR		load v3 source		
0000334A	E771 0000 0806		00000000	2547+	VL	v23, 0(R1)		use v22 to test decoder		
00003350	E756 7050 0E82			2548+	VFAE	V21, V22, V23, 0, 5		test instruction		
00003356	B98D 0020			2549+	EPSW	R2, R0		extract psw		
0000335A	5020 500C		0000000C	2550+	ST	R2, CCPSW		to save CC		
0000335E	E750 5040 080E		00003320	2551+	VST	V21, V1048		save v1 output		
00003364	07FB			2552+	BR	R11		return		
00003368				2553+RE48	DC	0F		V1 for this test		
00003368				2554+	DROP	R5				
00003368	00000000 00FF0000			2555	DC	XL16' 00000000 00FF0000 00000000 00000000'		V1		
00003370	00000000 00000000									
00003378	5D3A5859 5A255953			2556	DC	XL16'	5D3A5859 5A255953 54004D44 5F444546'	v2		
00003380	54004D44 5F444546									
00003388	25252525 25252525			2557	DC	XL16'	25252525 25252525 25252525 25252525'	v3		
00003390	25252525 25252525									
				2558						
				2559	* Byte, Equal before zero					
				2560	VRR_B	VFAE, 0, 13, 1		cc=1 M5=8+4+1	IN RT	CS
00003398				2561+	DS	0FD				
00003398		00003398		2562+	USING	*, R5		base for test data and test routine		
00003398	000033F0			2563+T49	DC	A(X49)		address of test routine		
0000339C	0031			2564+	DC	H' 49'		test number		
0000339E	00			2565+	DC	X' 00'				
0000339F	00			2566+	DC	HL1' 0'		m4 used		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000033A0	0D			2567+	DC	HL1' 13'	m5 used		
000033A1	01			2568+	DC	HL1' 1'	CC		
000033A2	0B			2569+	DC	HL1' 11'	CC failed mask		
000033A4	00000000 00000000			2570+	DS	2F	extracted PSW after test (has CC)		
000033AC	FF			2571+	DC	X' FF'	extracted CC, if test failed		
000033AD	E5C6C1C5 40404040			2572+	DC	CL8' VFAE'	instruction name		
000033B8	00003420			2573+	DC	A(RE49)	address of v1 result		
000033BC	00003430			2574+	DC	A(RE49+16)	address of v2 source		
000033C0	00003440			2575+	DC	A(RE49+32)	address of v3 source		
000033C4	00000010			2576+	DC	A(16)	result length		
000033C8	00003420			2577+REA49	DC	A(RE49)	result address		
000033D0	00000000 00000000			2578+	DS	FD	gap		
000033D8	00000000 00000000			2579+V1049	DS	XL16	V1 output		
000033E0	00000000 00000000								
000033E8	00000000 00000000			2580+	DS	FD	gap		
				2581+*					
000033F0				2582+X49	DS	0F			
000033F0	E310 5024 0014		00000024	2583+	LGF	R1, V2ADDR	load v2 source		
000033F6	E761 0000 0806		00000000	2584+	VL	v22, 0(R1)	use v21 to test decoder		
000033FC	E310 5028 0014		00000028	2585+	LGF	R1, V3ADDR	load v3 source		
00003402	E771 0000 0806		00000000	2586+	VL	v23, 0(R1)	use v22 to test decoder		
00003408	E756 70D0 0E82			2587+	VFAE	V21, V22, V23, 0, 13	test instruction		
0000340E	B98D 0020			2588+	EPSW	R2, R0	extract psw		
00003412	5020 500C		0000000C	2589+	ST	R2, CCPSW	to save CC		
00003416	E750 5040 080E		000033D8	2590+	VST	V21, V1049	save v1 output		
0000341C	07FB			2591+	BR	R11	return		
00003420				2592+RE49	DC	0F	V1 for this test		
00003420				2593+	DROP	R5			
00003420	FFFFFFFF FF00FFFF			2594	DC	XL16' FFFFFFFFFF FF00FFFF FFFFFFFFFF FFFFFFFFFF'	V1		
00003428	FFFFFFFF FFFFFFFFFF								
00003430	5D3A5859 5A255953			2595	DC	XL16' 5D3A5859 5A255953 54004D44 5F444546'	v2		
00003438	54004D44 5F444546								
00003440	25252525 25252525			2596	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003448	25252525 25252525								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2598 *-----	
				2599 * Byte Equal after zero	
00003450				2600 VRR_B VFAE, 0, 3, 0	cc=0 M5=2+1 ZS CS
00003450		00003450		2601+ DS OFD	
00003450	000034A8			2602+ USING *, R5	base for test data and test routine
00003454	0032			2603+T50 DC A(X50)	address of test routine
00003456	00			2604+ DC H' 50'	test number
00003457	00			2605+ DC X' 00'	
00003458	03			2606+ DC HL1' 0'	m4 used
00003459	00			2607+ DC HL1' 3'	m5 used
0000345A	07			2608+ DC HL1' 0'	CC
0000345C	00000000 00000000			2609+ DC HL1' 7'	CC failed mask
00003464	FF			2610+ DS 2F	extracted PSW after test (has CC)
00003465	E5C6C1C5 40404040			2611+ DC X' FF'	extracted CC, if test failed
00003470	000034D8			2612+ DC CL8' VFAE'	instruction name
00003474	000034E8			2613+ DC A(RE50)	address of v1 result
00003478	000034F8			2614+ DC A(RE50+16)	address of v2 source
0000347C	00000010			2615+ DC A(RE50+32)	address of v3 source
00003480	000034D8			2616+ DC A(16)	result length
00003488	00000000 00000000			2617+REA50 DC A(RE50)	result address
00003490	00000000 00000000			2618+ DS FD	gap
00003498	00000000 00000000			2619+V1050 DS XL16	V1 output
000034A0	00000000 00000000			2620+ DS FD	gap
				2621+*	
000034A8				2622+X50 DS OF	
000034A8	E310 5024 0014	00000024		2623+ LGF R1, V2ADDR	load v2 source
000034AE	E761 0000 0806	00000000		2624+ VL v22, 0(R1)	use v21 to test decoder
000034B4	E310 5028 0014	00000028		2625+ LGF R1, V3ADDR	load v3 source
000034BA	E771 0000 0806	00000000		2626+ VL v23, 0(R1)	use v22 to test decoder
000034C0	E756 7030 0E82			2627+ VFAE V21, V22, V23, 0, 3	test instruction
000034C6	B98D 0020			2628+ EPSW R2, R0	extract psw
000034CA	5020 500C	0000000C		2629+ ST R2, CCPSW	to save CC
000034CE	E750 5040 080E	00003490		2630+ VST V21, V1050	save v1 output
000034D4	07FB			2631+ BR R11	return
000034D8				2632+RE50 DC OF	V1 for this test
000034D8				2633+ DROP R5	
000034D8	00000000 00000005			2634 DC XL16' 00000000 00000005 00000000 00000000'	V1
000034E0	00000000 00000000				
000034E8	5D3A5859 5A005953		2635	DC XL16' 5D3A5859 5A005953 54254D44 5F444546'	v2
000034F0	54254D44 5F444546				
000034F8	25252525 25252525		2636	DC XL16' 25252525 25252525 25252525 25252525'	v3
00003500	25252525 25252525				
				2637	
				2638 * Byte Equal after zero	
00003508				2639 VRR_B VFAE, 0, 7, 0	cc=0 M5=4+2+1 RT ZS CS
00003508		00003508		2640+ DS OFD	
00003508	00003560			2641+ USING *, R5	base for test data and test routine
0000350C	0033			2642+T51 DC A(X51)	address of test routine
0000350E	00			2643+ DC H' 51'	test number
0000350F	00			2644+ DC X' 00'	
00003510	07			2645+ DC HL1' 0'	m4 used
00003511	00			2646+ DC HL1' 7'	m5 used
00003512	07			2647+ DC HL1' 0'	CC
00003514	00000000 00000000			2648+ DC HL1' 7'	CC failed mask
				2649+ DS 2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000351C	FF			2650+	DC	X' FF'
0000351D	E5C6C1C5 40404040			2651+	DC	CL8' VFAE'
00003528	00003590			2652+	DC	A(RE51)
0000352C	000035A0			2653+	DC	A(RE51+16)
00003530	000035B0			2654+	DC	A(RE51+32)
00003534	00000010			2655+	DC	A(16)
00003538	00003590			2656+REA51	DC	A(RE51)
00003540	00000000 00000000			2657+	DS	FD
00003548	00000000 00000000			2658+V1051	DS	XL16
00003550	00000000 00000000					
00003558	00000000 00000000			2659+	DS	FD
				2660+*		
00003560				2661+X51	DS	OF
00003560	E310 5024 0014		00000024	2662+	LGF	R1, V2ADDR
00003566	E761 0000 0806		00000000	2663+	VL	v22, 0(R1)
0000356C	E310 5028 0014		00000028	2664+	LGF	R1, V3ADDR
00003572	E771 0000 0806		00000000	2665+	VL	v23, 0(R1)
00003578	E756 7070 0E82			2666+	VFAE	V21, V22, V23, 0, 7
0000357E	B98D 0020			2667+	EPSW	R2, R0
00003582	5020 500C		0000000C	2668+	ST	R2, CCPSW
00003586	E750 5040 080E		00003548	2669+	VST	V21, V1051
0000358C	07FB			2670+	BR	R11
00003590				2671+RE51	DC	OF
00003590				2672+	DROP	R5
00003590	00000000 00000000			2673	DC	XL16' 00000000 00000000 00FF0000 00000000'
00003598	00FF0000 00000000					V1
000035A0	5D3A5859 5A005953			2674	DC	XL16' 5D3A5859 5A005953 54254D44 5F444546'
000035A8	54254D44 5F444546					v2
000035B0	25252525 25252525			2675	DC	XL16' 25252525 25252525 25252525 25252525'
000035B8	25252525 25252525					v3
				2676		
				2677 * Byte Equal after zero		
				2678	VRR_B	VFAE, 0, 15, 2
000035C0				2679+	DS	OFD
000035C0		000035C0		2680+	USING	*, R5
000035C0	00003618			2681+T52	DC	A(X52)
000035C4	0034			2682+	DC	H' 52'
000035C6	00			2683+	DC	X' 00'
000035C7	00			2684+	DC	HL1' 0'
000035C8	0F			2685+	DC	HL1' 15'
000035C9	02			2686+	DC	HL1' 2'
000035CA	0D			2687+	DC	HL1' 13'
000035CC	00000000 00000000			2688+	DS	2F
000035D4	FF			2689+	DC	X' FF'
000035D5	E5C6C1C5 40404040			2690+	DC	CL8' VFAE'
000035E0	00003648			2691+	DC	A(RE52)
000035E4	00003658			2692+	DC	A(RE52+16)
000035E8	00003668			2693+	DC	A(RE52+32)
000035EC	00000010			2694+	DC	A(16)
000035F0	00003648			2695+REA52	DC	A(RE52)
000035F8	00000000 00000000			2696+	DS	FD
00003600	00000000 00000000			2697+V1052	DS	XL16
00003608	00000000 00000000					
00003610	00000000 00000000			2698+	DS	FD
				2699+*		
00003618				2700+X52	DS	OF



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003618	E310 5024 0014		00000024	2701+	LGF	R1, V2ADDR	load v2 source		
0000361E	E761 0000 0806		00000000	2702+	VL	v22, 0(R1)	use v21 to test decoder		
00003624	E310 5028 0014		00000028	2703+	LGF	R1, V3ADDR	load v3 source		
0000362A	E771 0000 0806		00000000	2704+	VL	v23, 0(R1)	use v22 to test decoder		
00003630	E756 70F0 0E82			2705+	VFAE	V21, V22, V23, 0, 15	test instruction		
00003636	B98D 0020			2706+	EPSW	R2, R0	extract psw		
0000363A	5020 500C		0000000C	2707+	ST	R2, CCPSW	to save CC		
0000363E	E750 5040 080E		00003600	2708+	VST	V21, V1052	save v1 output		
00003644	07FB			2709+	BR	R11	return		
00003648				2710+RE52	DC	0F	V1 for this test		
00003648				2711+	DROP	R5			
00003648	FFFFFFFF FFFFFFFF			2712	DC	XL16' FFFFFFFF FFFFFFFF FF00FFFF FFFFFFFF'	V1		
00003650	FF00FFFF FFFFFFFF								
00003658	5D3A5859 5A005953			2713	DC	XL16' 5D3A5859 5A005953 54254D44 5F444546'	v2		
00003660	54254D44 5F444546								
00003668	25252525 25252525			2714	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003670	25252525 25252525								
				2715					
				2716 * Byte Equal after zero					
				2717	VRR_B	VFAE, 0, 1, 1	cc=1 M5=1	CS	
00003678				2718+	DS	0FD			
00003678		00003678		2719+	USING	*, R5	base for test data and test routine		
00003678	000036D0			2720+T53	DC	A(X53)	address of test routine		
0000367C	0035			2721+	DC	H' 53'	test number		
0000367E	00			2722+	DC	X' 00'			
0000367F	00			2723+	DC	HL1' 0'	m4 used		
00003680	01			2724+	DC	HL1' 1'	m5 used		
00003681	01			2725+	DC	HL1' 1'	CC		
00003682	0B			2726+	DC	HL1' 11'	CC failed mask		
00003684	00000000 00000000			2727+	DS	2F	extracted PSW after test (has CC)		
0000368C	FF			2728+	DC	X' FF'	extracted CC, if test failed		
0000368D	E5C6C1C5 40404040			2729+	DC	CL8' VFAE'	instruction name		
00003698	00003700			2730+	DC	A(RE53)	address of v1 result		
0000369C	00003710			2731+	DC	A(RE53+16)	address of v2 source		
000036A0	00003720			2732+	DC	A(RE53+32)	address of v3 source		
000036A4	00000010			2733+	DC	A(16)	result length		
000036A8	00003700			2734+REA53	DC	A(RE53)	result address		
000036B0	00000000 00000000			2735+	DS	FD	gap		
000036B8	00000000 00000000			2736+V1053	DS	XL16	V1 output		
000036C0	00000000 00000000								
000036C8	00000000 00000000			2737+	DS	FD	gap		
				2738+*					
000036D0				2739+X53	DS	0F			
000036D0	E310 5024 0014		00000024	2740+	LGF	R1, V2ADDR	load v2 source		
000036D6	E761 0000 0806		00000000	2741+	VL	v22, 0(R1)	use v21 to test decoder		
000036DC	E310 5028 0014		00000028	2742+	LGF	R1, V3ADDR	load v3 source		
000036E2	E771 0000 0806		00000000	2743+	VL	v23, 0(R1)	use v22 to test decoder		
000036E8	E756 7010 0E82			2744+	VFAE	V21, V22, V23, 0, 1	test instruction		
000036EE	B98D 0020			2745+	EPSW	R2, R0	extract psw		
000036F2	5020 500C		0000000C	2746+	ST	R2, CCPSW	to save CC		
000036F6	E750 5040 080E		000036B8	2747+	VST	V21, V1053	save v1 output		
000036FC	07FB			2748+	BR	R11	return		
00003700				2749+RE53	DC	0F	V1 for this test		
00003700				2750+	DROP	R5			
00003700	00000000 00000009			2751	DC	XL16' 00000000 00000009 00000000 00000000'	V1		
00003708	00000000 00000000								



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00003710	5D3A5859 5A005953			2752	DC	XL16'	5D3A5859 5A005953 54254D44 5F444546'	v2		
00003718	54254D44 5F444546									
00003720	25252525 25252525			2753	DC	XL16'	25252525 25252525 25252525 25252525'	v3		
00003728	25252525 25252525									
				2754						
				2755	* Byte Equal after zero					
				2756	VRR_B	VFAE, 0, 5, 1	cc=1 M5=4+1	RT	CS	
00003730				2757+	DS	OFD				
00003730		00003730		2758+	USING	*, R5	base for test data and test routine			
00003730	00003788			2759+T54	DC	A(X54)	address of test routine			
00003734	0036			2760+	DC	H' 54'	test number			
00003736	00			2761+	DC	X' 00'				
00003737	00			2762+	DC	HL1' 0'	m4 used			
00003738	05			2763+	DC	HL1' 5'	m5 used			
00003739	01			2764+	DC	HL1' 1'	CC			
0000373A	0B			2765+	DC	HL1' 11'	CC failed mask			
0000373C	00000000 00000000			2766+	DS	2F	extracted PSW after test (has CC)			
00003744	FF			2767+	DC	X' FF'	extracted CC, if test failed			
00003745	E5C6C1C5 40404040			2768+	DC	CL8' VFAE'	instruction name			
00003750	000037B8			2769+	DC	A(RE54)	address of v1 result			
00003754	000037C8			2770+	DC	A(RE54+16)	address of v2 source			
00003758	000037D8			2771+	DC	A(RE54+32)	address of v3 source			
0000375C	00000010			2772+	DC	A(16)	result length			
00003760	000037B8			2773+REA54	DC	A(RE54)	result address			
00003768	00000000 00000000			2774+	DS	FD	gap			
00003770	00000000 00000000			2775+V1054	DS	XL16	V1 output			
00003778	00000000 00000000									
00003780	00000000 00000000			2776+	DS	FD	gap			
				2777+*						
00003788				2778+X54	DS	OF				
00003788	E310 5024 0014		00000024	2779+	LGF	R1, V2ADDR	load v2 source			
0000378E	E761 0000 0806		00000000	2780+	VL	v22, 0(R1)	use v21 to test decoder			
00003794	E310 5028 0014		00000028	2781+	LGF	R1, V3ADDR	load v3 source			
0000379A	E771 0000 0806		00000000	2782+	VL	v23, 0(R1)	use v22 to test decoder			
000037A0	E756 7050 0E82			2783+	VFAE	V21, V22, V23, 0, 5	test instruction			
000037A6	B98D 0020			2784+	EPSW	R2, R0	extract psw			
000037AA	5020 500C		0000000C	2785+	ST	R2, CCPSW	to save CC			
000037AE	E750 5040 080E		00003770	2786+	VST	V21, V1054	save v1 output			
000037B4	07FB			2787+	BR	R11	return			
000037B8				2788+RE54	DC	OF	V1 for this test			
000037B8				2789+	DROP	R5				
000037B8	00000000 00000000			2790	DC	XL16' 00000000 00000000 00FF0000 00000000'	V1			
000037C0	00FF0000 00000000									
000037C8	5D3A5859 5A005953			2791	DC	XL16' 5D3A5859 5A005953 54254D44 5F444546'	v2			
000037D0	54254D44 5F444546									
000037D8	25252525 25252525			2792	DC	XL16' 25252525 25252525 25252525 25252525'	v3			
000037E0	25252525 25252525									
				2793						
				2794	* Byte Equal after zero					
				2795	VRR_B	VFAE, 0, 13, 1	cc=1 M5=8+4+1	IN RT	CS	
000037E8				2796+	DS	OFD				
000037E8		000037E8		2797+	USING	*, R5	base for test data and test routine			
000037E8	00003840			2798+T55	DC	A(X55)	address of test routine			
000037EC	0037			2799+	DC	H' 55'	test number			
000037EE	00			2800+	DC	X' 00'				
000037EF	00			2801+	DC	HL1' 0'	m4 used			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000037F0	0D			2802+	DC	HL1' 13'	m5 used		
000037F1	01			2803+	DC	HL1' 1'	CC		
000037F2	0B			2804+	DC	HL1' 11'	CC failed mask		
000037F4	00000000 00000000			2805+	DS	2F	extracted PSW after test (has CC)		
000037FC	FF			2806+	DC	X' FF'	extracted CC, if test failed		
000037FD	E5C6C1C5 40404040			2807+	DC	CL8' VFAE'	instruction name		
00003808	00003870			2808+	DC	A(RE55)	address of v1 result		
0000380C	00003880			2809+	DC	A(RE55+16)	address of v2 source		
00003810	00003890			2810+	DC	A(RE55+32)	address of v3 source		
00003814	00000010			2811+	DC	A(16)	result length		
00003818	00003870			2812+REA55	DC	A(RE55)	result address		
00003820	00000000 00000000			2813+	DS	FD	gap		
00003828	00000000 00000000			2814+V1055	DS	XL16	V1 output		
00003830	00000000 00000000								
00003838	00000000 00000000			2815+	DS	FD	gap		
				2816+*					
00003840				2817+X55	DS	0F			
00003840	E310 5024 0014		00000024	2818+	LGF	R1, V2ADDR	load v2 source		
00003846	E761 0000 0806		00000000	2819+	VL	v22, 0(R1)	use v21 to test decoder		
0000384C	E310 5028 0014		00000028	2820+	LGF	R1, V3ADDR	load v3 source		
00003852	E771 0000 0806		00000000	2821+	VL	v23, 0(R1)	use v22 to test decoder		
00003858	E756 70D0 0E82			2822+	VFAE	V21, V22, V23, 0, 13	test instruction		
0000385E	B98D 0020			2823+	EPSW	R2, R0	extract psw		
00003862	5020 500C		0000000C	2824+	ST	R2, CCPSW	to save CC		
00003866	E750 5040 080E		00003828	2825+	VST	V21, V1055	save v1 output		
0000386C	07FB			2826+	BR	R11	return		
00003870				2827+RE55	DC	0F	V1 for this test		
00003870				2828+	DROP	R5			
00003870	FFFFFFFF FFFFFFFF			2829	DC	XL16' FFFFFFFF FFFFFFFF FF00FFFF FFFFFFFF'	V1		
00003878	FF00FFFF FFFFFFFF								
00003880	5D3A5859 5A005953			2830	DC	XL16' 5D3A5859 5A005953 54254D44 5F444546'	v2		
00003888	54254D44 5F444546								
00003890	25252525 25252525			2831	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003898	25252525 25252525								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2833 *-----	
				2834 * Halfword, No equal, no zero	
000038A0				2835 VRR_B VFAE, 1, 3, 3	cc=3 M5=2+1 ZS CS
000038A0		000038A0		2836+ DS OFD	
000038A0	000038F8			2837+ USING *, R5	base for test data and test routine
000038A4	0038			2838+T56 DC A(X56)	address of test routine
000038A6	00			2839+ DC H' 56'	test number
000038A7	01			2840+ DC X' 00'	
000038A8	03			2841+ DC HL1' 1'	m4 used
000038A9	03			2842+ DC HL1' 3'	m5 used
000038AA	0E			2843+ DC HL1' 3'	CC
000038AC	00000000 00000000			2844+ DC HL1' 14'	CC failed mask
000038B4	FF			2845+ DS 2F	extracted PSW after test (has CC)
000038B5	E5C6C1C5 40404040			2846+ DC X' FF'	extracted CC, if test failed
000038C0	00003928			2847+ DC CL8' VFAE'	instruction name
000038C4	00003938			2848+ DC A(RE56)	address of v1 result
000038C8	00003948			2849+ DC A(RE56+16)	address of v2 source
000038CC	00000010			2850+ DC A(RE56+32)	address of v3 source
000038D0	00003928			2851+ DC A(16)	result length
000038D8	00000000 00000000			2852+REA56 DC A(RE56)	result address
000038E0	00000000 00000000			2853+ DS FD	gap
000038E8	00000000 00000000			2854+V1056 DS XL16	V1 output
000038F0	00000000 00000000			2855+ DS FD	gap
				2856+*	
000038F8				2857+X56 DS OF	
000038F8	E310 5024 0014	00000024		2858+ LGF R1, V2ADDR	load v2 source
000038FE	E761 0000 0806	00000000		2859+ VL v22, 0(R1)	use v21 to test decoder
00003904	E310 5028 0014	00000028		2860+ LGF R1, V3ADDR	load v3 source
0000390A	E771 0000 0806	00000000		2861+ VL v23, 0(R1)	use v22 to test decoder
00003910	E756 7030 1E82			2862+ VFAE V21, V22, V23, 1, 3	test instruction
00003916	B98D 0020			2863+ EPSW R2, R0	extract psw
0000391A	5020 500C	0000000C		2864+ ST R2, CCPSW	to save CC
0000391E	E750 5040 080E	000038E0		2865+ VST V21, V1056	save v1 output
00003924	07FB			2866+ BR R11	return
00003928				2867+RE56 DC OF	V1 for this test
00003928				2868+ DROP R5	
00003928	00000000 00000010			2869 DC XL16' 00000000 00000010 00000000 00000000'	V1
00003930	00000000 00000000				
00003938	5D3A5859 5A535953		2870	DC XL16' 5D3A5859 5A535953 54454D44 5F444546'	v2
00003940	54454D44 5F444546				
00003948	25252525 25252525		2871	DC XL16' 25252525 25252525 25252525 25252525'	v3
00003950	25252525 25252525				
				2872	
				2873 * Halfword, No equal, no zero	
00003958				2874 VRR_B VFAE, 1, 7, 3	cc=3 M5=4+2+1 RT ZS CS
00003958		00003958		2875+ DS OFD	
00003958	000039B0			2876+ USING *, R5	base for test data and test routine
0000395C	0039			2877+T57 DC A(X57)	address of test routine
0000395E	00			2878+ DC H' 57'	test number
0000395F	01			2879+ DC X' 00'	
00003960	07			2880+ DC HL1' 1'	m4 used
00003961	03			2881+ DC HL1' 7'	m5 used
00003962	0E			2882+ DC HL1' 3'	CC
00003964	00000000 00000000			2883+ DC HL1' 14'	CC failed mask
				2884+ DS 2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000396C	FF			2885+	DC	X' FF'	extracted CC, if test failed		
0000396D	E5C6C1C5 40404040			2886+	DC	CL8' VFAE'	instruction name		
00003978	000039E0			2887+	DC	A(RE57)	address of v1 result		
0000397C	000039F0			2888+	DC	A(RE57+16)	address of v2 source		
00003980	00003A00			2889+	DC	A(RE57+32)	address of v3 source		
00003984	00000010			2890+	DC	A(16)	result length		
00003988	000039E0			2891+REA57	DC	A(RE57)	result address		
00003990	00000000 00000000			2892+	DS	FD	gap		
00003998	00000000 00000000			2893+V1057	DS	XL16	V1 output		
000039A0	00000000 00000000								
000039A8	00000000 00000000			2894+	DS	FD	gap		
				2895+*					
000039B0				2896+X57	DS	0F			
000039B0	E310 5024 0014		00000024	2897+	LGF	R1, V2ADDR	load v2 source		
000039B6	E761 0000 0806		00000000	2898+	VL	v22, 0(R1)	use v21 to test decoder		
000039BC	E310 5028 0014		00000028	2899+	LGF	R1, V3ADDR	load v3 source		
000039C2	E771 0000 0806		00000000	2900+	VL	v23, 0(R1)	use v22 to test decoder		
000039C8	E756 7070 1E82			2901+	VFAE	V21, V22, V23, 1, 7	test instruction		
000039CE	B98D 0020			2902+	EPSW	R2, R0	extract psw		
000039D2	5020 500C		0000000C	2903+	ST	R2, CCPSW	to save CC		
000039D6	E750 5040 080E		00003998	2904+	VST	V21, V1057	save v1 output		
000039DC	07FB			2905+	BR	R11	return		
000039E0				2906+RE57	DC	0F	V1 for this test		
000039E0				2907+	DROP	R5			
000039E0	00000000 00000000			2908	DC	XL16' 00000000 00000000 00000000 00000000'	V1		
000039E8	00000000 00000000								
000039F0	5D3A5859 5A535953			2909	DC	XL16' 5D3A5859 5A535953 54454D44 5F444546'	v2		
000039F8	54454D44 5F444546								
00003A00	25252525 25252525			2910	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003A08	25252525 25252525								
				2911					
				2912 * Halfword, No		equal, no zero			
				2913	VRR_B	VFAE, 1, 15, 1	cc=1 M5=8+4+2+1 IN RT ZS CS		
00003A10				2914+	DS	0FD			
00003A10		00003A10		2915+	USING	*, R5	base for test data and test routine		
00003A10	00003A68			2916+T58	DC	A(X58)	address of test routine		
00003A14	003A			2917+	DC	H' 58'	test number		
00003A16	00			2918+	DC	X' 00'			
00003A17	01			2919+	DC	HL1' 1'	m4 used		
00003A18	0F			2920+	DC	HL1' 15'	m5 used		
00003A19	01			2921+	DC	HL1' 1'	CC		
00003A1A	0B			2922+	DC	HL1' 11'	CC failed mask		
00003A1C	00000000 00000000			2923+	DS	2F	extracted PSW after test (has CC)		
00003A24	FF			2924+	DC	X' FF'	extracted CC, if test failed		
00003A25	E5C6C1C5 40404040			2925+	DC	CL8' VFAE'	instruction name		
00003A30	00003A98			2926+	DC	A(RE58)	address of v1 result		
00003A34	00003AA8			2927+	DC	A(RE58+16)	address of v2 source		
00003A38	00003AB8			2928+	DC	A(RE58+32)	address of v3 source		
00003A3C	00000010			2929+	DC	A(16)	result length		
00003A40	00003A98			2930+REA58	DC	A(RE58)	result address		
00003A48	00000000 00000000			2931+	DS	FD	gap		
00003A50	00000000 00000000			2932+V1058	DS	XL16	V1 output		
00003A58	00000000 00000000								
00003A60	00000000 00000000			2933+	DS	FD	gap		
				2934+*					
00003A68				2935+X58	DS	0F			



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003A68	E310 5024 0014		00000024	2936+	LGF	R1, V2ADDR	load v2 source		
00003A6E	E761 0000 0806		00000000	2937+	VL	v22, 0(R1)	use v21 to test decoder		
00003A74	E310 5028 0014		00000028	2938+	LGF	R1, V3ADDR	load v3 source		
00003A7A	E771 0000 0806		00000000	2939+	VL	v23, 0(R1)	use v22 to test decoder		
00003A80	E756 70F0 1E82			2940+	VFAE	V21, V22, V23, 1, 15	test instruction		
00003A86	B98D 0020			2941+	EPSW	R2, R0	extract psw		
00003A8A	5020 500C		0000000C	2942+	ST	R2, CCPSW	to save CC		
00003A8E	E750 5040 080E		00003A50	2943+	VST	V21, V1058	save v1 output		
00003A94	07FB			2944+	BR	R11	return		
00003A98				2945+RE58	DC	0F	V1 for this test		
00003A98				2946+	DROP	R5			
00003A98	FFFFFFFF FFFFFFFF			2947	DC	XL16' FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'	V1		
00003AA0	FFFFFFFF FFFFFFFF								
00003AA8	5D3A5859 5A535953			2948	DC	XL16' 5D3A5859 5A535953 54454D44 5F444546'	v2		
00003AB0	54454D44 5F444546								
00003AB8	25252525 25252525			2949	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003AC0	25252525 25252525								
				2950					
				2951 *	Halfword, Equal, no zero				
				2952	VRR_B VFAE, 1, 3, 1		cc=1 M5=2+1	ZS CS	
00003AC8				2953+	DS	0FD			
00003AC8		00003AC8		2954+	USING	*, R5	base for test data and test routine		
00003AC8	00003B20			2955+T59	DC	A(X59)	address of test routine		
00003ACC	003B			2956+	DC	H' 59'	test number		
00003ACE	00			2957+	DC	X' 00'			
00003ACF	01			2958+	DC	HL1' 1'	m4 used		
00003AD0	03			2959+	DC	HL1' 3'	m5 used		
00003AD1	01			2960+	DC	HL1' 1'	CC		
00003AD2	0B			2961+	DC	HL1' 11'	CC failed mask		
00003AD4	00000000 00000000			2962+	DS	2F	extracted PSW after test (has CC)		
00003ADC	FF			2963+	DC	X' FF'	extracted CC, if test failed		
00003ADD	E5C6C1C5 40404040			2964+	DC	CL8' VFAE'	instruction name		
00003AE8	00003B50			2965+	DC	A(RE59)	address of v1 result		
00003AEC	00003B60			2966+	DC	A(RE59+16)	address of v2 source		
00003AF0	00003B70			2967+	DC	A(RE59+32)	address of v3 source		
00003AF4	00000010			2968+	DC	A(16)	result length		
00003AF8	00003B50			2969+REA59	DC	A(RE59)	result address		
00003B00	00000000 00000000			2970+	DS	FD	gap		
00003B08	00000000 00000000			2971+V1059	DS	XL16	V1 output		
00003B10	00000000 00000000								
00003B18	00000000 00000000			2972+	DS	FD	gap		
				2973+*					
00003B20				2974+X59	DS	0F			
00003B20	E310 5024 0014		00000024	2975+	LGF	R1, V2ADDR	load v2 source		
00003B26	E761 0000 0806		00000000	2976+	VL	v22, 0(R1)	use v21 to test decoder		
00003B2C	E310 5028 0014		00000028	2977+	LGF	R1, V3ADDR	load v3 source		
00003B32	E771 0000 0806		00000000	2978+	VL	v23, 0(R1)	use v22 to test decoder		
00003B38	E756 7030 1E82			2979+	VFAE	V21, V22, V23, 1, 3	test instruction		
00003B3E	B98D 0020			2980+	EPSW	R2, R0	extract psw		
00003B42	5020 500C		0000000C	2981+	ST	R2, CCPSW	to save CC		
00003B46	E750 5040 080E		00003B08	2982+	VST	V21, V1059	save v1 output		
00003B4C	07FB			2983+	BR	R11	return		
00003B50				2984+RE59	DC	0F	V1 for this test		
00003B50				2985+	DROP	R5			
00003B50	00000000 00000006			2986	DC	XL16' 00000000 00000006 00000000 00000000'	V1		
00003B58	00000000 00000000								



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00003B60	5D3A5859 5A532525			2987	DC	XL16'	5D3A5859 5A532525 54454D44 5F444546'	v2		
00003B68	54454D44 5F444546									
00003B70	25252525 25252525			2988	DC	XL16'	25252525 25252525 25252525 25252525'	v3		
00003B78	25252525 25252525									
				2989						
				2990	* Halfword, Equal, no zero					
				2991	VRR_B	VFAE, 1, 7, 1	cc=1 M5=4+2+1	RT ZS CS		
00003B80				2992+	DS	OFD				
00003B80		00003B80		2993+	USING	*, R5	base for test data and test routine			
00003B80	00003BD8			2994+T60	DC	A(X60)	address of test routine			
00003B84	003C			2995+	DC	H' 60'	test number			
00003B86	00			2996+	DC	X' 00'				
00003B87	01			2997+	DC	HL1' 1'	m4 used			
00003B88	07			2998+	DC	HL1' 7'	m5 used			
00003B89	01			2999+	DC	HL1' 1'	CC			
00003B8A	0B			3000+	DC	HL1' 11'	CC failed mask			
00003B8C	00000000 00000000			3001+	DS	2F	extracted PSW after test (has CC)			
00003B94	FF			3002+	DC	X' FF'	extracted CC, if test failed			
00003B95	E5C6C1C5 40404040			3003+	DC	CL8' VFAE'	instruction name			
00003BA0	00003C08			3004+	DC	A(RE60)	address of v1 result			
00003BA4	00003C18			3005+	DC	A(RE60+16)	address of v2 source			
00003BA8	00003C28			3006+	DC	A(RE60+32)	address of v3 source			
00003BAC	00000010			3007+	DC	A(16)	result length			
00003BB0	00003C08			3008+REA60	DC	A(RE60)	result address			
00003BB8	00000000 00000000			3009+	DS	FD	gap			
00003BC0	00000000 00000000			3010+V1060	DS	XL16	V1 output			
00003BC8	00000000 00000000									
00003BD0	00000000 00000000			3011+	DS	FD	gap			
				3012+*						
00003BD8				3013+X60	DS	OF				
00003BD8	E310 5024 0014		00000024	3014+	LGF	R1, V2ADDR	load v2 source			
00003BDE	E761 0000 0806		00000000	3015+	VL	v22, 0(R1)	use v21 to test decoder			
00003BE4	E310 5028 0014		00000028	3016+	LGF	R1, V3ADDR	load v3 source			
00003BEA	E771 0000 0806		00000000	3017+	VL	v23, 0(R1)	use v22 to test decoder			
00003BF0	E756 7070 1E82			3018+	VFAE	V21, V22, V23, 1, 7	test instruction			
00003BF6	B98D 0020			3019+	EPSW	R2, R0	extract psw			
00003BFA	5020 500C		0000000C	3020+	ST	R2, CCPSW	to save CC			
00003BFE	E750 5040 080E		00003BC0	3021+	VST	V21, V1060	save v1 output			
00003C04	07FB			3022+	BR	R11	return			
00003C08				3023+RE60	DC	OF	V1 for this test			
00003C08				3024+	DROP	R5				
00003C08	00000000 0000FFFF			3025	DC	XL16' 00000000 0000FFFF 00000000 00000000'	V1			
00003C10	00000000 00000000									
00003C18	5D3A5859 5A532525			3026	DC	XL16' 5D3A5859 5A532525 54454D44 5F444546'	v2			
00003C20	54454D44 5F444546									
00003C28	25252525 25252525			3027	DC	XL16' 25252525 25252525 25252525 25252525'	v3			
00003C30	25252525 25252525									
				3028						
				3029	* Halfword, Equal, no zero					
				3030	VRR_B	VFAE, 1, 15, 1	cc=1 M5=8+4+2+1	IN RT ZS CS		
00003C38				3031+	DS	OFD				
00003C38		00003C38		3032+	USING	*, R5	base for test data and test routine			
00003C38	00003C90			3033+T61	DC	A(X61)	address of test routine			
00003C3C	003D			3034+	DC	H' 61'	test number			
00003C3E	00			3035+	DC	X' 00'				
00003C3F	01			3036+	DC	HL1' 1'	m4 used			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003C40	0F			3037+	DC	HL1' 15'	m5 used		
00003C41	01			3038+	DC	HL1' 1'	CC		
00003C42	0B			3039+	DC	HL1' 11'	CC failed mask		
00003C44	00000000 00000000			3040+	DS	2F	extracted PSW after test (has CC)		
00003C4C	FF			3041+	DC	X' FF'	extracted CC, if test failed		
00003C4D	E5C6C1C5 40404040			3042+	DC	CL8' VFAE'	instruction name		
00003C58	00003CC0			3043+	DC	A(RE61)	address of v1 result		
00003C5C	00003CD0			3044+	DC	A(RE61+16)	address of v2 source		
00003C60	00003CE0			3045+	DC	A(RE61+32)	address of v3 source		
00003C64	00000010			3046+	DC	A(16)	result length		
00003C68	00003CC0			3047+REA61	DC	A(RE61)	result address		
00003C70	00000000 00000000			3048+	DS	FD	gap		
00003C78	00000000 00000000			3049+V1061	DS	XL16	V1 output		
00003C80	00000000 00000000								
00003C88	00000000 00000000			3050+	DS	FD	gap		
				3051+*					
00003C90				3052+X61	DS	0F			
00003C90	E310 5024 0014		00000024	3053+	LGF	R1, V2ADDR	load v2 source		
00003C96	E761 0000 0806		00000000	3054+	VL	v22, 0(R1)	use v21 to test decoder		
00003C9C	E310 5028 0014		00000028	3055+	LGF	R1, V3ADDR	load v3 source		
00003CA2	E771 0000 0806		00000000	3056+	VL	v23, 0(R1)	use v22 to test decoder		
00003CA8	E756 70F0 1E82			3057+	VFAE	V21, V22, V23, 1, 15	test instruction		
00003CAE	B98D 0020			3058+	EPSW	R2, R0	extract psw		
00003CB2	5020 500C		0000000C	3059+	ST	R2, CCPSW	to save CC		
00003CB6	E750 5040 080E		00003C78	3060+	VST	V21, V1061	save v1 output		
00003CBC	07FB			3061+	BR	R11	return		
00003CC0				3062+RE61	DC	0F	V1 for this test		
00003CC0				3063+	DROP	R5			
00003CC0	FFFFFFFF FFFF0000			3064	DC	XL16' FFFFFFFFFF FFFF0000 FFFFFFFFFF FFFFFFFFFF'	V1		
00003CC8	FFFFFFFF FFFFFFFFFF								
00003CD0	5D3A5859 5A532525			3065	DC	XL16' 5D3A5859 5A532525 54454D44 5F444546'	v2		
00003CD8	54454D44 5F444546								
00003CE0	25252525 25252525			3066	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003CE8	25252525 25252525								
				3067					
				3068 * Halfword, Equal before zero					
				3069	VRR_B	VFAE, 1, 3, 2	cc=2 M5=2+1	ZS CS	
00003CF0				3070+	DS	0FD			
00003CF0		00003CF0		3071+	USING	*, R5	base for test data and test routine		
00003CF0	00003D48			3072+T62	DC	A(X62)	address of test routine		
00003CF4	003E			3073+	DC	H' 62'	test number		
00003CF6	00			3074+	DC	X' 00'			
00003CF7	01			3075+	DC	HL1' 1'	m4 used		
00003CF8	03			3076+	DC	HL1' 3'	m5 used		
00003CF9	02			3077+	DC	HL1' 2'	CC		
00003CFA	0D			3078+	DC	HL1' 13'	CC failed mask		
00003CFC	00000000 00000000			3079+	DS	2F	extracted PSW after test (has CC)		
00003D04	FF			3080+	DC	X' FF'	extracted CC, if test failed		
00003D05	E5C6C1C5 40404040			3081+	DC	CL8' VFAE'	instruction name		
00003D10	00003D78			3082+	DC	A(RE62)	address of v1 result		
00003D14	00003D88			3083+	DC	A(RE62+16)	address of v2 source		
00003D18	00003D98			3084+	DC	A(RE62+32)	address of v3 source		
00003D1C	00000010			3085+	DC	A(16)	result length		
00003D20	00003D78			3086+REA62	DC	A(RE62)	result address		
00003D28	00000000 00000000			3087+	DS	FD	gap		
00003D30	00000000 00000000			3088+V1062	DS	XL16	V1 output		



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00003E30				3140+RE63	DC	0F	V1 for this test			
00003E30				3141+	DROP	R5				
00003E30	00000000	0000FFFF		3142	DC	XL16'	00000000	0000FFFF	00000000	00000000'
00003E38	00000000	00000000								V1
00003E40	5D3A5859	5A532525		3143	DC	XL16'	5D3A5859	5A532525	54450000	5F444546'
00003E48	54450000	5F444546								v2
00003E50	25252525	25252525		3144	DC	XL16'	25252525	25252525	25252525	25252525'
00003E58	25252525	25252525								v3
				3145						
				3146	* Halfword, Equal before zero					
				3147	VRR_B	VFAE, 1, 15, 2	cc=2 M5=8+4+2+1 IN RT ZS CS			
00003E60				3148+	DS	0FD				
00003E60			00003E60	3149+	USING	*, R5	base for test data and test routine			
00003E60	00003EB8			3150+T64	DC	A(X64)	address of test routine			
00003E64	0040			3151+	DC	H' 64'	test number			
00003E66	00			3152+	DC	X' 00'				
00003E67	01			3153+	DC	HL1' 1'	m4 used			
00003E68	0F			3154+	DC	HL1' 15'	m5 used			
00003E69	02			3155+	DC	HL1' 2'	CC			
00003E6A	0D			3156+	DC	HL1' 13'	CC failed mask			
00003E6C	00000000	00000000		3157+	DS	2F	extracted PSW after test (has CC)			
00003E74	FF			3158+	DC	X' FF'	extracted CC, if test failed			
00003E75	E5C6C1C5	40404040		3159+	DC	CL8' VFAE'	instruction name			
00003E80	00003EE8			3160+	DC	A(RE64)	address of v1 result			
00003E84	00003EF8			3161+	DC	A(RE64+16)	address of v2 source			
00003E88	00003F08			3162+	DC	A(RE64+32)	address of v3 source			
00003E8C	00000010			3163+	DC	A(16)	result length			
00003E90	00003EE8			3164+REA64	DC	A(RE64)	result address			
00003E98	00000000	00000000		3165+	DS	FD	gap			
00003EA0	00000000	00000000		3166+V1064	DS	XL16	V1 output			
00003EA8	00000000	00000000								
00003EB0	00000000	00000000		3167+	DS	FD	gap			
				3168+*						
00003EB8				3169+X64	DS	0F				
00003EB8	E310 5024 0014		00000024	3170+	LGF	R1, V2ADDR	load v2 source			
00003EBE	E761 0000 0806		00000000	3171+	VL	v22, 0(R1)	use v21 to test decoder			
00003EC4	E310 5028 0014		00000028	3172+	LGF	R1, V3ADDR	load v3 source			
00003ECA	E771 0000 0806		00000000	3173+	VL	v23, 0(R1)	use v22 to test decoder			
00003ED0	E756 70F0 1E82			3174+	VFAE	V21, V22, V23, 1, 15	test instruction			
00003ED6	B98D 0020			3175+	EPSW	R2, R0	extract psw			
00003EDA	5020 500C		0000000C	3176+	ST	R2, CCPSW	to save CC			
00003EDE	E750 5040 080E		00003EA0	3177+	VST	V21, V1064	save v1 output			
00003EE4	07FB			3178+	BR	R11	return			
00003EE8				3179+RE64	DC	0F	V1 for this test			
00003EE8				3180+	DROP	R5				
00003EE8	FFFFFFFF	FFFF0000		3181	DC	XL16'	FFFFFFFF	FFFF0000	FFFFFFFF	FFFFFFFF'
00003EF0	FFFFFFFF	FFFFFFFF								V1
00003EF8	5D3A5859	5A532525		3182	DC	XL16'	5D3A5859	5A532525	54450000	5F444546'
00003F00	54450000	5F444546								v2
00003F08	25252525	25252525		3183	DC	XL16'	25252525	25252525	25252525	25252525'
00003F10	25252525	25252525								v3
				3184						
				3185	* Halfword, Equal after zero					
				3186	VRR_B	VFAE, 1, 3, 0	cc=0 M5=2+1 ZS CS			
00003F18				3187+	DS	0FD				
00003F18			00003F18	3188+	USING	*, R5	base for test data and test routine			



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003F18	00003F70			3189+T65	DC	A(X65)	address of test routine		
00003F1C	0041			3190+	DC	H' 65'	test number		
00003F1E	00			3191+	DC	X' 00'			
00003F1F	01			3192+	DC	HL1' 1'	m4 used		
00003F20	03			3193+	DC	HL1' 3'	m5 used		
00003F21	00			3194+	DC	HL1' 0'	CC		
00003F22	07			3195+	DC	HL1' 7'	CC failed mask		
00003F24	00000000 00000000			3196+	DS	2F	extracted PSW after test (has CC)		
00003F2C	FF			3197+	DC	X' FF'	extracted CC, if test failed		
00003F2D	E5C6C1C5 40404040			3198+	DC	CL8' VFAE'	instruction name		
00003F38	00003FA0			3199+	DC	A(RE65)	address of v1 result		
00003F3C	00003FB0			3200+	DC	A(RE65+16)	address of v2 source		
00003F40	00003FC0			3201+	DC	A(RE65+32)	address of v3 source		
00003F44	00000010			3202+	DC	A(16)	result length		
00003F48	00003FA0			3203+REA65	DC	A(RE65)	result address		
00003F50	00000000 00000000			3204+	DS	FD	gap		
00003F58	00000000 00000000			3205+V1065	DS	XL16	V1 output		
00003F60	00000000 00000000								
00003F68	00000000 00000000			3206+	DS	FD	gap		
				3207+*					
00003F70				3208+X65	DS	0F			
00003F70	E310 5024 0014		00000024	3209+	LGF	R1, V2ADDR	load v2 source		
00003F76	E761 0000 0806		00000000	3210+	VL	v22, 0(R1)	use v21 to test decoder		
00003F7C	E310 5028 0014		00000028	3211+	LGF	R1, V3ADDR	load v3 source		
00003F82	E771 0000 0806		00000000	3212+	VL	v23, 0(R1)	use v22 to test decoder		
00003F88	E756 7030 1E82			3213+	VFAE	V21, V22, V23, 1, 3	test instruction		
00003F8E	B98D 0020			3214+	EPSW	R2, R0	extract psw		
00003F92	5020 500C		0000000C	3215+	ST	R2, CCPSW	to save CC		
00003F96	E750 5040 080E		00003F58	3216+	VST	V21, V1065	save v1 output		
00003F9C	07FB			3217+	BR	R11	return		
00003FA0				3218+RE65	DC	0F	V1 for this test		
00003FA0				3219+	DROP	R5			
00003FA0	00000000 00000006			3220	DC	XL16' 00000000 00000006 00000000 00000000'	V1		
00003FA8	00000000 00000000								
00003FB0	5D3A5859 5A530000			3221	DC	XL16' 5D3A5859 5A530000 54452525 5F444546'	v2		
00003FB8	54452525 5F444546								
00003FC0	25252525 25252525			3222	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00003FC8	25252525 25252525								
				3223					
				3224 * Halfword, Equal after zero					
				3225	VRR_B	VFAE, 1, 7, 0	cc=0 M5=4+2+1 RT ZS CS		
00003FD0				3226+	DS	0FD			
00003FD0		00003FD0		3227+	USING	*, R5	base for test data and test routine		
00003FD0	00004028			3228+T66	DC	A(X66)	address of test routine		
00003FD4	0042			3229+	DC	H' 66'	test number		
00003FD6	00			3230+	DC	X' 00'			
00003FD7	01			3231+	DC	HL1' 1'	m4 used		
00003FD8	07			3232+	DC	HL1' 7'	m5 used		
00003FD9	00			3233+	DC	HL1' 0'	CC		
00003FDA	07			3234+	DC	HL1' 7'	CC failed mask		
00003FDC	00000000 00000000			3235+	DS	2F	extracted PSW after test (has CC)		
00003FE4	FF			3236+	DC	X' FF'	extracted CC, if test failed		
00003FE5	E5C6C1C5 40404040			3237+	DC	CL8' VFAE'	instruction name		
00003FF0	00004058			3238+	DC	A(RE66)	address of v1 result		
00003FF4	00004068			3239+	DC	A(RE66+16)	address of v2 source		
00003FF8	00004078			3240+	DC	A(RE66+32)	address of v3 source		



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003FFC	00000010			3241+	DC	A(16)		result length	
00004000	00004058			3242+REA66	DC	A(RE66)		result address	
00004008	00000000 00000000			3243+	DS	FD		gap	
00004010	00000000 00000000			3244+V1066	DS	XL16		V1 output	
00004018	00000000 00000000								
00004020	00000000 00000000			3245+	DS	FD		gap	
				3246+*					
00004028				3247+X66	DS	OF			
00004028	E310 5024 0014		00000024	3248+	LGF	R1, V2ADDR		load v2 source	
0000402E	E761 0000 0806		00000000	3249+	VL	v22, 0(R1)		use v21 to test decoder	
00004034	E310 5028 0014		00000028	3250+	LGF	R1, V3ADDR		load v3 source	
0000403A	E771 0000 0806		00000000	3251+	VL	v23, 0(R1)		use v22 to test decoder	
00004040	E756 7070 1E82			3252+	VFAE	V21, V22, V23, 1, 7		test instruction	
00004046	B98D 0020			3253+	EPSW	R2, R0		extract psw	
0000404A	5020 500C		0000000C	3254+	ST	R2, CCPSW		to save CC	
0000404E	E750 5040 080E		00004010	3255+	VST	V21, V1066		save v1 output	
00004054	07FB			3256+	BR	R11		return	
00004058				3257+RE66	DC	OF		V1 for this test	
00004058				3258+	DROP	R5			
00004058	00000000 00000000			3259	DC	XL16' 00000000 00000000 0000FFFF 00000000'		V1	
00004060	0000FFFF 00000000								
00004068	5D3A5859 5A530000			3260	DC	XL16' 5D3A5859 5A530000 54452525 5F444546'		v2	
00004070	54452525 5F444546								
00004078	25252525 25252525			3261	DC	XL16' 25252525 25252525 25252525 25252525'		v3	
00004080	25252525 25252525								
				3262					
				3263 * Halfword, Equal after zero					
				3264	VRR_B	VFAE, 1, 15, 2		cc=2 M5=8+4+2+1 IN RT ZS CS	
00004088				3265+	DS	OFD			
00004088		00004088		3266+	USING	*, R5		base for test data and test routine	
00004088	000040E0			3267+T67	DC	A(X67)		address of test routine	
0000408C	0043			3268+	DC	H' 67'		test number	
0000408E	00			3269+	DC	X' 00'			
0000408F	01			3270+	DC	HL1' 1'		m4 used	
00004090	0F			3271+	DC	HL1' 15'		m5 used	
00004091	02			3272+	DC	HL1' 2'		CC	
00004092	0D			3273+	DC	HL1' 13'		CC failed mask	
00004094	00000000 00000000			3274+	DS	2F		extracted PSW after test (has CC)	
0000409C	FF			3275+	DC	X' FF'		extracted CC, if test failed	
0000409D	E5C6C1C5 40404040			3276+	DC	CL8' VFAE'		instruction name	
000040A8	00004110			3277+	DC	A(RE67)		address of v1 result	
000040AC	00004120			3278+	DC	A(RE67+16)		address of v2 source	
000040B0	00004130			3279+	DC	A(RE67+32)		address of v3 source	
000040B4	00000010			3280+	DC	A(16)		result length	
000040B8	00004110			3281+REA67	DC	A(RE67)		result address	
000040C0	00000000 00000000			3282+	DS	FD		gap	
000040C8	00000000 00000000			3283+V1067	DS	XL16		V1 output	
000040D0	00000000 00000000								
000040D8	00000000 00000000			3284+	DS	FD		gap	
				3285+*					
000040E0				3286+X67	DS	OF			
000040E0	E310 5024 0014		00000024	3287+	LGF	R1, V2ADDR		load v2 source	
000040E6	E761 0000 0806		00000000	3288+	VL	v22, 0(R1)		use v21 to test decoder	
000040EC	E310 5028 0014		00000028	3289+	LGF	R1, V3ADDR		load v3 source	
000040F2	E771 0000 0806		00000000	3290+	VL	v23, 0(R1)		use v22 to test decoder	
000040F8	E756 70F0 1E82			3291+	VFAE	V21, V22, V23, 1, 15		test instruction	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3302 *	-----
				3303 *	Word, No equal, no zero
				3304	VRR_B VFAE, 2, 3, 3 cc=3 M5=2+1 ZS CS
00004140				3305+	DS OFD
00004140		00004140		3306+	USING *, R5 base for test data and test routine
00004140	00004198			3307+T68	DC A(X68) address of test routine
00004144	0044			3308+	DC H' 68' test number
00004146	00			3309+	DC X' 00'
00004147	02			3310+	DC HL1' 2' m4 used
00004148	03			3311+	DC HL1' 3' m5 used
00004149	03			3312+	DC HL1' 3' CC
0000414A	0E			3313+	DC HL1' 14' CC failed mask
0000414C	00000000 00000000			3314+	DS 2F extracted PSW after test (has CC)
00004154	FF			3315+	DC X' FF' extracted CC, if test failed
00004155	E5C6C1C5 40404040			3316+	DC CL8' VFAE' instruction name
00004160	000041C8			3317+	DC A(RE68) address of v1 result
00004164	000041D8			3318+	DC A(RE68+16) address of v2 source
00004168	000041E8			3319+	DC A(RE68+32) address of v3 source
0000416C	00000010			3320+	DC A(16) result length
00004170	000041C8			3321+REA68	DC A(RE68) result address
00004178	00000000 00000000			3322+	DS FD gap
00004180	00000000 00000000			3323+V1068	DS XL16 V1 output
00004188	00000000 00000000				
00004190	00000000 00000000			3324+	DS FD gap
				3325+*	
00004198				3326+X68	DS OF
00004198	E310 5024 0014		00000024	3327+	LGF R1, V2ADDR load v2 source
0000419E	E761 0000 0806		00000000	3328+	VL v22, 0(R1) use v21 to test decoder
000041A4	E310 5028 0014		00000028	3329+	LGF R1, V3ADDR load v3 source
000041AA	E771 0000 0806		00000000	3330+	VL v23, 0(R1) use v22 to test decoder
000041B0	E756 7030 2E82			3331+	VFAE V21, V22, V23, 2, 3 test instruction
000041B6	B98D 0020			3332+	EPSW R2, R0 extract psw
000041BA	5020 500C		0000000C	3333+	ST R2, CCPSW to save CC
000041BE	E750 5040 080E		00004180	3334+	VST V21, V1068 save v1 output
000041C4	07FB			3335+	BR R11 return
000041C8				3336+RE68	DC OF V1 for this test
000041C8				3337+	DROP R5
000041C8	00000000 00000010			3338	DC XL16' 00000000 00000010 00000000 00000000' V1
000041D0	00000000 00000000				
000041D8	5D3A5859 5A535953			3339	DC XL16' 5D3A5859 5A535953 54454D44 5F444546' v2
000041E0	54454D44 5F444546				
000041E8	25252525 25252525			3340	DC XL16' 25252525 25252525 25252525 25252525' v3
000041F0	25252525 25252525				
				3341	
				3342 *	Word, No equal, no zero
				3343	VRR_B VFAE, 2, 7, 3 cc=3 M5=4+2+1 RT ZS CS
000041F8				3344+	DS OFD
000041F8		000041F8		3345+	USING *, R5 base for test data and test routine
000041F8	00004250			3346+T69	DC A(X69) address of test routine
000041FC	0045			3347+	DC H' 69' test number
000041FE	00			3348+	DC X' 00'
000041FF	02			3349+	DC HL1' 2' m4 used
00004200	07			3350+	DC HL1' 7' m5 used
00004201	03			3351+	DC HL1' 3' CC
00004202	0E			3352+	DC HL1' 14' CC failed mask
00004204	00000000 00000000			3353+	DS 2F extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000420C	FF			3354+	DC	X' FF'	extracted CC, if test failed		
0000420D	E5C6C1C5 40404040			3355+	DC	CL8' VFAE'	instruction name		
00004218	00004280			3356+	DC	A(RE69)	address of v1 result		
0000421C	00004290			3357+	DC	A(RE69+16)	address of v2 source		
00004220	000042A0			3358+	DC	A(RE69+32)	address of v3 source		
00004224	00000010			3359+	DC	A(16)	result length		
00004228	00004280			3360+REA69	DC	A(RE69)	result address		
00004230	00000000 00000000			3361+	DS	FD	gap		
00004238	00000000 00000000			3362+V1069	DS	XL16	V1 output		
00004240	00000000 00000000								
00004248	00000000 00000000			3363+	DS	FD	gap		
				3364+*					
00004250				3365+X69	DS	0F			
00004250	E310 5024 0014		00000024	3366+	LGF	R1, V2ADDR	load v2 source		
00004256	E761 0000 0806		00000000	3367+	VL	v22, 0(R1)	use v21 to test decoder		
0000425C	E310 5028 0014		00000028	3368+	LGF	R1, V3ADDR	load v3 source		
00004262	E771 0000 0806		00000000	3369+	VL	v23, 0(R1)	use v22 to test decoder		
00004268	E756 7070 2E82			3370+	VFAE	V21, V22, V23, 2, 7	test instruction		
0000426E	B98D 0020			3371+	EPSW	R2, R0	extract psw		
00004272	5020 500C		0000000C	3372+	ST	R2, CCPSW	to save CC		
00004276	E750 5040 080E		00004238	3373+	VST	V21, V1069	save v1 output		
0000427C	07FB			3374+	BR	R11	return		
00004280				3375+RE69	DC	0F	V1 for this test		
00004280				3376+	DROP	R5			
00004280	00000000 00000000			3377	DC	XL16' 00000000 00000000 00000000 00000000'	V1		
00004288	00000000 00000000								
00004290	5D3A5859 5A535953			3378	DC	XL16' 5D3A5859 5A535953 54454D44 5F444546'	v2		
00004298	54454D44 5F444546								
000042A0	25252525 25252525			3379	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
000042A8	25252525 25252525								
				3380					
				3381 * Word, No equal, no zero					
				3382	VRR_B	VFAE, 2, 15, 1	cc=1 M5=8+4+2+1 IN RT ZS CS		
000042B0				3383+	DS	0FD			
000042B0		000042B0		3384+	USING	*, R5	base for test data and test routine		
000042B0	00004308			3385+T70	DC	A(X70)	address of test routine		
000042B4	0046			3386+	DC	H' 70'	test number		
000042B6	00			3387+	DC	X' 00'			
000042B7	02			3388+	DC	HL1' 2'	m4 used		
000042B8	0F			3389+	DC	HL1' 15'	m5 used		
000042B9	01			3390+	DC	HL1' 1'	CC		
000042BA	0B			3391+	DC	HL1' 11'	CC failed mask		
000042BC	00000000 00000000			3392+	DS	2F	extracted PSW after test (has CC)		
000042C4	FF			3393+	DC	X' FF'	extracted CC, if test failed		
000042C5	E5C6C1C5 40404040			3394+	DC	CL8' VFAE'	instruction name		
000042D0	00004338			3395+	DC	A(RE70)	address of v1 result		
000042D4	00004348			3396+	DC	A(RE70+16)	address of v2 source		
000042D8	00004358			3397+	DC	A(RE70+32)	address of v3 source		
000042DC	00000010			3398+	DC	A(16)	result length		
000042E0	00004338			3399+REA70	DC	A(RE70)	result address		
000042E8	00000000 00000000			3400+	DS	FD	gap		
000042F0	00000000 00000000			3401+V1070	DS	XL16	V1 output		
000042F8	00000000 00000000								
00004300	00000000 00000000			3402+	DS	FD	gap		
				3403+*					
00004308				3404+X70	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004308	E310 5024 0014		00000024	3405+	LGF	R1, V2ADDR	load v2 source		
0000430E	E761 0000 0806		00000000	3406+	VL	v22, 0(R1)	use v21 to test decoder		
00004314	E310 5028 0014		00000028	3407+	LGF	R1, V3ADDR	load v3 source		
0000431A	E771 0000 0806		00000000	3408+	VL	v23, 0(R1)	use v22 to test decoder		
00004320	E756 70F0 2E82			3409+	VFAE	V21, V22, V23, 2, 15	test instruction		
00004326	B98D 0020			3410+	EPSW	R2, R0	extract psw		
0000432A	5020 500C		0000000C	3411+	ST	R2, CCPSW	to save CC		
0000432E	E750 5040 080E		000042F0	3412+	VST	V21, V1070	save v1 output		
00004334	07FB			3413+	BR	R11	return		
00004338				3414+RE70	DC	0F	V1 for this test		
00004338				3415+	DROP	R5			
00004338	FFFFFFFF FFFFFFFF			3416	DC	XL16' FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'	V1		
00004340	FFFFFFFF FFFFFFFF								
00004348	5D3A5859 5A535953			3417	DC	XL16' 5D3A5859 5A535953 54454D44 5F444546'	v2		
00004350	54454D44 5F444546								
00004358	25252525 25252525			3418	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00004360	25252525 25252525								
				3419					
				3420 * Word, Equal, no zero					
				3421	VRR_B	VFAE, 2, 3, 1	cc=1 M5=2+1	ZS CS	
00004368				3422+	DS	0FD			
00004368		00004368		3423+	USING	*, R5	base for test data and test routine		
00004368	000043C0			3424+T71	DC	A(X71)	address of test routine		
0000436C	0047			3425+	DC	H' 71'	test number		
0000436E	00			3426+	DC	X' 00'			
0000436F	02			3427+	DC	HL1' 2'	m4 used		
00004370	03			3428+	DC	HL1' 3'	m5 used		
00004371	01			3429+	DC	HL1' 1'	CC		
00004372	0B			3430+	DC	HL1' 11'	CC failed mask		
00004374	00000000 00000000			3431+	DS	2F	extracted PSW after test (has CC)		
0000437C	FF			3432+	DC	X' FF'	extracted CC, if test failed		
0000437D	E5C6C1C5 40404040			3433+	DC	CL8' VFAE'	instruction name		
00004388	000043F0			3434+	DC	A(RE71)	address of v1 result		
0000438C	00004400			3435+	DC	A(RE71+16)	address of v2 source		
00004390	00004410			3436+	DC	A(RE71+32)	address of v3 source		
00004394	00000010			3437+	DC	A(16)	result length		
00004398	000043F0			3438+REA71	DC	A(RE71)	result address		
000043A0	00000000 00000000			3439+	DS	FD	gap		
000043A8	00000000 00000000			3440+V1071	DS	XL16	V1 output		
000043B0	00000000 00000000								
000043B8	00000000 00000000			3441+	DS	FD	gap		
				3442+*					
000043C0				3443+X71	DS	0F			
000043C0	E310 5024 0014		00000024	3444+	LGF	R1, V2ADDR	load v2 source		
000043C6	E761 0000 0806		00000000	3445+	VL	v22, 0(R1)	use v21 to test decoder		
000043CC	E310 5028 0014		00000028	3446+	LGF	R1, V3ADDR	load v3 source		
000043D2	E771 0000 0806		00000000	3447+	VL	v23, 0(R1)	use v22 to test decoder		
000043D8	E756 7030 2E82			3448+	VFAE	V21, V22, V23, 2, 3	test instruction		
000043DE	B98D 0020			3449+	EPSW	R2, R0	extract psw		
000043E2	5020 500C		0000000C	3450+	ST	R2, CCPSW	to save CC		
000043E6	E750 5040 080E		000043A8	3451+	VST	V21, V1071	save v1 output		
000043EC	07FB			3452+	BR	R11	return		
000043F0				3453+RE71	DC	0F	V1 for this test		
000043F0				3454+	DROP	R5			
000043F0	00000000 00000004			3455	DC	XL16' 00000000 00000004 00000000 00000000'	V1		
000043F8	00000000 00000000								



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00004400	5D3A5859	25252525		3456	DC	XL16'	5D3A5859	25252525	54454D44	5F444546' v2
00004408	54454D44	5F444546								
00004410	25252525	25252525		3457	DC	XL16'	25252525	25252525	25252525	25252525' v3
00004418	25252525	25252525								
				3458						
				3459	* Word, Equal, no zero					
				3460	VRR_B VFAE, 2, 7, 1			cc=1	M5=4+2+1	RT ZS CS
00004420				3461+	DS	OFD				
00004420			00004420	3462+	USING	*, R5				base for test data and test routine
00004420	00004478			3463+T72	DC	A(X72)				address of test routine
00004424	0048			3464+	DC	H' 72'				test number
00004426	00			3465+	DC	X' 00'				
00004427	02			3466+	DC	HL1' 2'			m4 used	
00004428	07			3467+	DC	HL1' 7'			m5 used	
00004429	01			3468+	DC	HL1' 1'			CC	
0000442A	0B			3469+	DC	HL1' 11'			CC failed mask	
0000442C	00000000	00000000		3470+	DS	2F			extracted PSW after test (has CC)	
00004434	FF			3471+	DC	X' FF'			extracted CC, if test failed	
00004435	E5C6C1C5	40404040		3472+	DC	CL8' VFAE'			instruction name	
00004440	000044A8			3473+	DC	A(RE72)			address of v1 result	
00004444	000044B8			3474+	DC	A(RE72+16)			address of v2 source	
00004448	000044C8			3475+	DC	A(RE72+32)			address of v3 source	
0000444C	00000010			3476+	DC	A(16)			result length	
00004450	000044A8			3477+REA72	DC	A(RE72)			result address	
00004458	00000000	00000000		3478+	DS	FD			gap	
00004460	00000000	00000000		3479+V1072	DS	XL16			V1 output	
00004468	00000000	00000000								
00004470	00000000	00000000		3480+	DS	FD			gap	
				3481+*						
00004478				3482+X72	DS	OF				
00004478	E310 5024 0014		00000024	3483+	LGF	R1, V2ADDR				load v2 source
0000447E	E761 0000 0806		00000000	3484+	VL	v22, 0(R1)				use v21 to test decoder
00004484	E310 5028 0014		00000028	3485+	LGF	R1, V3ADDR				load v3 source
0000448A	E771 0000 0806		00000000	3486+	VL	v23, 0(R1)				use v22 to test decoder
00004490	E756 7070 2E82			3487+	VFAE	V21, V22, V23, 2, 7				test instruction
00004496	B98D 0020			3488+	EPSW	R2, R0				extract psw
0000449A	5020 500C		0000000C	3489+	ST	R2, CCPSW				to save CC
0000449E	E750 5040 080E		00004460	3490+	VST	V21, V1072				save v1 output
000044A4	07FB			3491+	BR	R11				return
000044A8				3492+RE72	DC	OF				V1 for this test
000044A8				3493+	DROP	R5				
000044A8	00000000	FFFFFFFF		3494	DC	XL16'	00000000	FFFFFFFF	00000000	00000000' V1
000044B0	00000000	00000000								
000044B8	5D3A5859	25252525		3495	DC	XL16'	5D3A5859	25252525	54454D44	5F444546' v2
000044C0	54454D44	5F444546								
000044C8	25252525	25252525		3496	DC	XL16'	25252525	25252525	25252525	25252525' v3
000044D0	25252525	25252525								
				3497						
				3498	* Word, Equal, no zero					
				3499	VRR_B VFAE, 2, 15, 1			cc=1	M5=8+4+2+1	IN RT ZS CS
000044D8				3500+	DS	OFD				
000044D8			000044D8	3501+	USING	*, R5				base for test data and test routine
000044D8	00004530			3502+T73	DC	A(X73)				address of test routine
000044DC	0049			3503+	DC	H' 73'				test number
000044DE	00			3504+	DC	X' 00'				
000044DF	02			3505+	DC	HL1' 2'			m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000044E0	0F			3506+	DC	HL1' 15'	m5 used		
000044E1	01			3507+	DC	HL1' 1'	CC		
000044E2	0B			3508+	DC	HL1' 11'	CC failed mask		
000044E4	00000000 00000000			3509+	DS	2F	extracted PSW after test (has CC)		
000044EC	FF			3510+	DC	X' FF'	extracted CC, if test failed		
000044ED	E5C6C1C5 40404040			3511+	DC	CL8' VFAE'	instruction name		
000044F8	00004560			3512+	DC	A(RE73)	address of v1 result		
000044FC	00004570			3513+	DC	A(RE73+16)	address of v2 source		
00004500	00004580			3514+	DC	A(RE73+32)	address of v3 source		
00004504	00000010			3515+	DC	A(16)	result length		
00004508	00004560			3516+REA73	DC	A(RE73)	result address		
00004510	00000000 00000000			3517+	DS	FD	gap		
00004518	00000000 00000000			3518+V1073	DS	XL16	V1 output		
00004520	00000000 00000000								
00004528	00000000 00000000			3519+	DS	FD	gap		
				3520+*					
00004530				3521+X73	DS	0F			
00004530	E310 5024 0014		00000024	3522+	LGF	R1, V2ADDR	load v2 source		
00004536	E761 0000 0806		00000000	3523+	VL	v22, 0(R1)	use v21 to test decoder		
0000453C	E310 5028 0014		00000028	3524+	LGF	R1, V3ADDR	load v3 source		
00004542	E771 0000 0806		00000000	3525+	VL	v23, 0(R1)	use v22 to test decoder		
00004548	E756 70F0 2E82			3526+	VFAE	V21, V22, V23, 2, 15	test instruction		
0000454E	B98D 0020			3527+	EPSW	R2, R0	extract psw		
00004552	5020 500C		0000000C	3528+	ST	R2, CCPSW	to save CC		
00004556	E750 5040 080E		00004518	3529+	VST	V21, V1073	save v1 output		
0000455C	07FB			3530+	BR	R11	return		
00004560				3531+RE73	DC	0F	V1 for this test		
00004560				3532+	DROP	R5			
00004560	FFFFFFFF 00000000			3533	DC	XL16' FFFFFFFF 00000000 FFFFFFFF FFFFFFFF'	V1		
00004568	FFFFFFFF FFFFFFFF								
00004570	5D3A5859 25252525			3534	DC	XL16' 5D3A5859 25252525 54454D44 5F444546'	v2		
00004578	54454D44 5F444546								
00004580	25252525 25252525			3535	DC	XL16' 25252525 25252525 25252525 25252525'	v3		
00004588	25252525 25252525								
				3536					
				3537 * Word, Equal before zero					
				3538	VRR_B	VFAE, 2, 3, 2	cc=2 M5=2+1	ZS CS	
00004590				3539+	DS	0FD			
00004590		00004590		3540+	USING	*, R5	base for test data and test routine		
00004590	000045E8			3541+T74	DC	A(X74)	address of test routine		
00004594	004A			3542+	DC	H' 74'	test number		
00004596	00			3543+	DC	X' 00'			
00004597	02			3544+	DC	HL1' 2'	m4 used		
00004598	03			3545+	DC	HL1' 3'	m5 used		
00004599	02			3546+	DC	HL1' 2'	CC		
0000459A	0D			3547+	DC	HL1' 13'	CC failed mask		
0000459C	00000000 00000000			3548+	DS	2F	extracted PSW after test (has CC)		
000045A4	FF			3549+	DC	X' FF'	extracted CC, if test failed		
000045A5	E5C6C1C5 40404040			3550+	DC	CL8' VFAE'	instruction name		
000045B0	00004618			3551+	DC	A(RE74)	address of v1 result		
000045B4	00004628			3552+	DC	A(RE74+16)	address of v2 source		
000045B8	00004638			3553+	DC	A(RE74+32)	address of v3 source		
000045BC	00000010			3554+	DC	A(16)	result length		
000045C0	00004618			3555+REA74	DC	A(RE74)	result address		
000045C8	00000000 00000000			3556+	DS	FD	gap		
000045D0	00000000 00000000			3557+V1074	DS	XL16	V1 output		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
000045D8	00000000	00000000								
000045E0	00000000	00000000		3558+	DS	FD	gap			
				3559+*						
000045E8				3560+X74	DS	OF				
000045E8	E310 5024 0014		00000024	3561+	LGF	R1, V2ADDR	load v2 source			
000045EE	E761 0000 0806		00000000	3562+	VL	v22, 0(R1)	use v21 to test decoder			
000045F4	E310 5028 0014		00000028	3563+	LGF	R1, V3ADDR	load v3 source			
000045FA	E771 0000 0806		00000000	3564+	VL	v23, 0(R1)	use v22 to test decoder			
00004600	E756 7030 2E82			3565+	VFAE	V21, V22, V23, 2, 3	test instruction			
00004606	B98D 0020			3566+	EPSW	R2, R0	extract psw			
0000460A	5020 500C		0000000C	3567+	ST	R2, CCPSW	to save CC			
0000460E	E750 5040 080E		000045D0	3568+	VST	V21, V1074	save v1 output			
00004614	07FB			3569+	BR	R11	return			
00004618				3570+RE74	DC	OF	V1 for this test			
00004618				3571+	DROP	R5				
00004618	00000000	00000004		3572	DC	XL16' 00000000 00000004 00000000 00000000'	V1			
00004620	00000000	00000000								
00004628	5D3A5859	25252525		3573	DC	XL16' 5D3A5859 25252525 00000000 5F444546'	v2			
00004630	00000000	5F444546								
00004638	25252525	25252525		3574	DC	XL16' 25252525 25252525 25252525 25252525'	v3			
00004640	25252525	25252525								
				3575						
				3576 * Word, Equal before zero						
				3577	VRR_B	VFAE, 2, 7, 2	cc=2 M5=4+2+1 RT ZS CS			
00004648				3578+	DS	OFD				
00004648			00004648	3579+	USING	*, R5	base for test data and test routine			
00004648	000046A0			3580+T75	DC	A(X75)	address of test routine			
0000464C	004B			3581+	DC	H' 75'	test number			
0000464E	00			3582+	DC	X' 00'				
0000464F	02			3583+	DC	HL1' 2'	m4 used			
00004650	07			3584+	DC	HL1' 7'	m5 used			
00004651	02			3585+	DC	HL1' 2'	CC			
00004652	0D			3586+	DC	HL1' 13'	CC failed mask			
00004654	00000000	00000000		3587+	DS	2F	extracted PSW after test (has CC)			
0000465C	FF			3588+	DC	X' FF'	extracted CC, if test failed			
0000465D	E5C6C1C5	40404040		3589+	DC	CL8' VFAE'	instruction name			
00004668	000046D0			3590+	DC	A(RE75)	address of v1 result			
0000466C	000046E0			3591+	DC	A(RE75+16)	address of v2 source			
00004670	000046F0			3592+	DC	A(RE75+32)	address of v3 source			
00004674	00000010			3593+	DC	A(16)	result length			
00004678	000046D0			3594+REA75	DC	A(RE75)	result address			
00004680	00000000	00000000		3595+	DS	FD	gap			
00004688	00000000	00000000		3596+V1075	DS	XL16	V1 output			
00004690	00000000	00000000								
00004698	00000000	00000000		3597+	DS	FD	gap			
				3598+*						
000046A0				3599+X75	DS	OF				
000046A0	E310 5024 0014		00000024	3600+	LGF	R1, V2ADDR	load v2 source			
000046A6	E761 0000 0806		00000000	3601+	VL	v22, 0(R1)	use v21 to test decoder			
000046AC	E310 5028 0014		00000028	3602+	LGF	R1, V3ADDR	load v3 source			
000046B2	E771 0000 0806		00000000	3603+	VL	v23, 0(R1)	use v22 to test decoder			
000046B8	E756 7070 2E82			3604+	VFAE	V21, V22, V23, 2, 7	test instruction			
000046BE	B98D 0020			3605+	EPSW	R2, R0	extract psw			
000046C2	5020 500C		0000000C	3606+	ST	R2, CCPSW	to save CC			
000046C6	E750 5040 080E		00004688	3607+	VST	V21, V1075	save v1 output			
000046CC	07FB			3608+	BR	R11	return			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
000046D0				3609+RE75	DC	0F	V1 for this test			
000046D0				3610+	DROP	R5				
000046D0	00000000	FFFFFFFF		3611	DC	XL16'	00000000	FFFFFFFF	00000000	00000000' V1
000046D8	00000000	00000000								
000046E0	5D3A5859	25252525		3612	DC	XL16'	5D3A5859	25252525	00000000	5F444546' v2
000046E8	00000000	5F444546								
000046F0	25252525	25252525		3613	DC	XL16'	25252525	25252525	25252525	25252525' v3
000046F8	25252525	25252525								
				3614						
				3615 * Word, Equal before zero						
				3616	VRR_B	VFAE, 2, 15, 2		cc=2	M5=8+4+2+1	IN RT ZS CS
00004700				3617+	DS	0FD				
00004700			00004700	3618+	USING	*, R5				base for test data and test routine
00004700	00004758			3619+T76	DC	A(X76)				address of test routine
00004704	004C			3620+	DC	H' 76'				test number
00004706	00			3621+	DC	X' 00'				
00004707	02			3622+	DC	HL1' 2'			m4 used	
00004708	0F			3623+	DC	HL1' 15'			m5 used	
00004709	02			3624+	DC	HL1' 2'			CC	
0000470A	0D			3625+	DC	HL1' 13'			CC failed mask	
0000470C	00000000	00000000		3626+	DS	2F			extracted PSW after test (has CC)	
00004714	FF			3627+	DC	X' FF'			extracted CC, if test failed	
00004715	E5C6C1C5	40404040		3628+	DC	CL8' VFAE'			instruction name	
00004720	00004788			3629+	DC	A(RE76)			address of v1 result	
00004724	00004798			3630+	DC	A(RE76+16)			address of v2 source	
00004728	000047A8			3631+	DC	A(RE76+32)			address of v3 source	
0000472C	00000010			3632+	DC	A(16)			result length	
00004730	00004788			3633+REA76	DC	A(RE76)			result address	
00004738	00000000	00000000		3634+	DS	FD			gap	
00004740	00000000	00000000		3635+V1076	DS	XL16			V1 output	
00004748	00000000	00000000								
00004750	00000000	00000000		3636+	DS	FD			gap	
				3637+*						
00004758				3638+X76	DS	0F				
00004758	E310 5024 0014		00000024	3639+	LGF	R1, V2ADDR			load v2 source	
0000475E	E761 0000 0806		00000000	3640+	VL	v22, 0(R1)			use v21 to test decoder	
00004764	E310 5028 0014		00000028	3641+	LGF	R1, V3ADDR			load v3 source	
0000476A	E771 0000 0806		00000000	3642+	VL	v23, 0(R1)			use v22 to test decoder	
00004770	E756 70F0 2E82			3643+	VFAE	V21, V22, V23, 2, 15			test instruction	
00004776	B98D 0020			3644+	EPSW	R2, R0			extract psw	
0000477A	5020 500C		0000000C	3645+	ST	R2, CCPSW			to save CC	
0000477E	E750 5040 080E		00004740	3646+	VST	V21, V1076			save v1 output	
00004784	07FB			3647+	BR	R11			return	
00004788				3648+RE76	DC	0F			V1 for this test	
00004788				3649+	DROP	R5				
00004788	FFFFFFFF	00000000		3650	DC	XL16'	FFFFFFFF	00000000	FFFFFFFF	FFFFFFFF' V1
00004790	FFFFFFFF	FFFFFFFF								
00004798	5D3A5859	25252525		3651	DC	XL16'	5D3A5859	25252525	00000000	5F444546' v2
000047A0	00000000	5F444546								
000047A8	25252525	25252525		3652	DC	XL16'	25252525	25252525	25252525	25252525' v3
000047B0	25252525	25252525								
				3653						
				3654 * Word, Equal after zero						
				3655	VRR_B	VFAE, 2, 3, 0		cc=0	M5=2+1	ZS CS
000047B8				3656+	DS	0FD				
000047B8			000047B8	3657+	USING	*, R5				base for test data and test routine



LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
000047B8	00004810			3658+T77	DC	A(X77)			address of test routine	
000047BC	004D			3659+	DC	H' 77'			test number	
000047BE	00			3660+	DC	X' 00'				
000047BF	02			3661+	DC	HL1' 2'			m4 used	
000047C0	03			3662+	DC	HL1' 3'			m5 used	
000047C1	00			3663+	DC	HL1' 0'			CC	
000047C2	07			3664+	DC	HL1' 7'			CC failed mask	
000047C4	00000000 00000000			3665+	DS	2F			extracted PSW after test (has CC)	
000047CC	FF			3666+	DC	X' FF'			extracted CC, if test failed	
000047CD	E5C6C1C5 40404040			3667+	DC	CL8' VFAE'			instruction name	
000047D8	00004840			3668+	DC	A(RE77)			address of v1 result	
000047DC	00004850			3669+	DC	A(RE77+16)			address of v2 source	
000047E0	00004860			3670+	DC	A(RE77+32)			address of v3 source	
000047E4	00000010			3671+	DC	A(16)			result length	
000047E8	00004840			3672+REA77	DC	A(RE77)			result address	
000047F0	00000000 00000000			3673+	DS	FD			gap	
000047F8	00000000 00000000			3674+V1077	DS	XL16			V1 output	
00004800	00000000 00000000									
00004808	00000000 00000000			3675+	DS	FD			gap	
				3676+*						
00004810				3677+X77	DS	0F				
00004810	E310 5024 0014		00000024	3678+	LGF	R1, V2ADDR			load v2 source	
00004816	E761 0000 0806		00000000	3679+	VL	v22, 0(R1)			use v21 to test decoder	
0000481C	E310 5028 0014		00000028	3680+	LGF	R1, V3ADDR			load v3 source	
00004822	E771 0000 0806		00000000	3681+	VL	v23, 0(R1)			use v22 to test decoder	
00004828	E756 7030 2E82			3682+	VFAE	V21, V22, V23, 2, 3			test instruction	
0000482E	B98D 0020			3683+	EPSW	R2, R0			extract psw	
00004832	5020 500C		0000000C	3684+	ST	R2, CCPSW			to save CC	
00004836	E750 5040 080E		000047F8	3685+	VST	V21, V1077			save v1 output	
0000483C	07FB			3686+	BR	R11			return	
00004840				3687+RE77	DC	0F			V1 for this test	
00004840				3688+	DROP	R5				
00004840	00000000 00000004			3689	DC	XL16' 00000000 00000004 00000000 00000000'			V1	
00004848	00000000 00000000									
00004850	5D3A5859 00000000			3690	DC	XL16' 5D3A5859 00000000 25252525 5F444546'			v2	
00004858	25252525 5F444546									
00004860	25252525 25252525			3691	DC	XL16' 25252525 25252525 25252525 25252525'			v3	
00004868	25252525 25252525									
				3692						
				3693 * Word, Equal after zero						
				3694	VRR_B	VFAE, 2, 7, 0			cc=0 M5=4+2+1	RT ZS CS
00004870				3695+	DS	0FD				
00004870		00004870		3696+	USING	*, R5			base for test data and test routine	
00004870	000048C8			3697+T78	DC	A(X78)			address of test routine	
00004874	004E			3698+	DC	H' 78'			test number	
00004876	00			3699+	DC	X' 00'				
00004877	02			3700+	DC	HL1' 2'			m4 used	
00004878	07			3701+	DC	HL1' 7'			m5 used	
00004879	00			3702+	DC	HL1' 0'			CC	
0000487A	07			3703+	DC	HL1' 7'			CC failed mask	
0000487C	00000000 00000000			3704+	DS	2F			extracted PSW after test (has CC)	
00004884	FF			3705+	DC	X' FF'			extracted CC, if test failed	
00004885	E5C6C1C5 40404040			3706+	DC	CL8' VFAE'			instruction name	
00004890	000048F8			3707+	DC	A(RE78)			address of v1 result	
00004894	00004908			3708+	DC	A(RE78+16)			address of v2 source	
00004898	00004918			3709+	DC	A(RE78+32)			address of v3 source	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000489C	00000010			3710+	DC	A(16)		result length	
000048A0	000048F8			3711+REA78	DC	A(RE78)		result address	
000048A8	00000000 00000000			3712+	DS	FD		gap	
000048B0	00000000 00000000			3713+V1078	DS	XL16		V1 output	
000048B8	00000000 00000000								
000048C0	00000000 00000000			3714+	DS	FD		gap	
				3715+*					
000048C8				3716+X78	DS	OF			
000048C8	E310 5024 0014		00000024	3717+	LGF	R1, V2ADDR		load v2 source	
000048CE	E761 0000 0806		00000000	3718+	VL	v22, 0(R1)		use v21 to test decoder	
000048D4	E310 5028 0014		00000028	3719+	LGF	R1, V3ADDR		load v3 source	
000048DA	E771 0000 0806		00000000	3720+	VL	v23, 0(R1)		use v22 to test decoder	
000048E0	E756 7070 2E82			3721+	VFAE	V21, V22, V23, 2, 7		test instruction	
000048E6	B98D 0020			3722+	EPSW	R2, R0		extract psw	
000048EA	5020 500C		0000000C	3723+	ST	R2, CCPSW		to save CC	
000048EE	E750 5040 080E		000048B0	3724+	VST	V21, V1078		save v1 output	
000048F4	07FB			3725+	BR	R11		return	
000048F8				3726+RE78	DC	OF		V1 for this test	
000048F8				3727+	DROP	R5			
000048F8	00000000 00000000			3728	DC	XL16' 00000000 00000000 FFFFFFFF 00000000'		V1	
00004900	FFFFFFFF 00000000								
00004908	5D3A5859 00000000			3729	DC	XL16' 5D3A5859 00000000 25252525 5F444546'		v2	
00004910	25252525 5F444546								
00004918	25252525 25252525			3730	DC	XL16' 25252525 25252525 25252525 25252525'		v3	
00004920	25252525 25252525								
				3731					
				3732 * Word, Equal after zero					
				3733	VRR_B	VFAE, 2, 15, 2		cc=2 M5=8+4+2+1 IN RT ZS CS	
00004928				3734+	DS	OFD			
00004928		00004928		3735+	USING	*, R5		base for test data and test routine	
00004928	00004980			3736+T79	DC	A(X79)		address of test routine	
0000492C	004F			3737+	DC	H' 79'		test number	
0000492E	00			3738+	DC	X' 00'			
0000492F	02			3739+	DC	HL1' 2'		m4 used	
00004930	0F			3740+	DC	HL1' 15'		m5 used	
00004931	02			3741+	DC	HL1' 2'		CC	
00004932	0D			3742+	DC	HL1' 13'		CC failed mask	
00004934	00000000 00000000			3743+	DS	2F		extracted PSW after test (has CC)	
0000493C	FF			3744+	DC	X' FF'		extracted CC, if test failed	
0000493D	E5C6C1C5 40404040			3745+	DC	CL8' VFAE'		instruction name	
00004948	000049B0			3746+	DC	A(RE79)		address of v1 result	
0000494C	000049C0			3747+	DC	A(RE79+16)		address of v2 source	
00004950	000049D0			3748+	DC	A(RE79+32)		address of v3 source	
00004954	00000010			3749+	DC	A(16)		result length	
00004958	000049B0			3750+REA79	DC	A(RE79)		result address	
00004960	00000000 00000000			3751+	DS	FD		gap	
00004968	00000000 00000000			3752+V1079	DS	XL16		V1 output	
00004970	00000000 00000000								
00004978	00000000 00000000			3753+	DS	FD		gap	
				3754+*					
00004980				3755+X79	DS	OF			
00004980	E310 5024 0014		00000024	3756+	LGF	R1, V2ADDR		load v2 source	
00004986	E761 0000 0806		00000000	3757+	VL	v22, 0(R1)		use v21 to test decoder	
0000498C	E310 5028 0014		00000028	3758+	LGF	R1, V3ADDR		load v3 source	
00004992	E771 0000 0806		00000000	3759+	VL	v23, 0(R1)		use v22 to test decoder	
00004998	E756 70F0 2E82			3760+	VFAE	V21, V22, V23, 2, 15		test instruction	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				3776 *
				3777 * table of pointers to individual tests
				3778 *
000049E8				3779 E7TESTS DS OF
				3780 PTTABLE
000049E8				3781+TTABLE DS OF
000049E8	00001118			3782+ DC A(T1) test address
000049EC	000011D0			3783+ DC A(T2) test address
000049F0	00001288			3784+ DC A(T3) test address
000049F4	00001340			3785+ DC A(T4) test address
000049F8	000013F8			3786+ DC A(T5) test address
000049FC	000014B0			3787+ DC A(T6) test address
00004A00	00001568			3788+ DC A(T7) test address
00004A04	00001620			3789+ DC A(T8) test address
00004A08	000016D8			3790+ DC A(T9) test address
00004A0C	00001790			3791+ DC A(T10) test address
00004A10	00001848			3792+ DC A(T11) test address
00004A14	00001900			3793+ DC A(T12) test address
00004A18	000019B8			3794+ DC A(T13) test address
00004A1C	00001A70			3795+ DC A(T14) test address
00004A20	00001B28			3796+ DC A(T15) test address
00004A24	00001BE0			3797+ DC A(T16) test address
00004A28	00001C98			3798+ DC A(T17) test address
00004A2C	00001D50			3799+ DC A(T18) test address
00004A30	00001E08			3800+ DC A(T19) test address
00004A34	00001EC0			3801+ DC A(T20) test address
00004A38	00001F78			3802+ DC A(T21) test address
00004A3C	00002030			3803+ DC A(T22) test address
00004A40	000020E8			3804+ DC A(T23) test address
00004A44	000021A0			3805+ DC A(T24) test address
00004A48	00002258			3806+ DC A(T25) test address
00004A4C	00002310			3807+ DC A(T26) test address
00004A50	000023C8			3808+ DC A(T27) test address
00004A54	00002480			3809+ DC A(T28) test address
00004A58	00002538			3810+ DC A(T29) test address
00004A5C	000025F0			3811+ DC A(T30) test address
00004A60	000026A8			3812+ DC A(T31) test address
00004A64	00002760			3813+ DC A(T32) test address
00004A68	00002818			3814+ DC A(T33) test address
00004A6C	000028D0			3815+ DC A(T34) test address
00004A70	00002988			3816+ DC A(T35) test address
00004A74	00002A40			3817+ DC A(T36) test address
00004A78	00002AF8			3818+ DC A(T37) test address
00004A7C	00002BB0			3819+ DC A(T38) test address
00004A80	00002C68			3820+ DC A(T39) test address
00004A84	00002D20			3821+ DC A(T40) test address
00004A88	00002DD8			3822+ DC A(T41) test address
00004A8C	00002E90			3823+ DC A(T42) test address
00004A90	00002F48			3824+ DC A(T43) test address
00004A94	00003000			3825+ DC A(T44) test address
00004A98	000030B8			3826+ DC A(T45) test address
00004A9C	00003170			3827+ DC A(T46) test address
00004AA0	00003228			3828+ DC A(T47) test address
00004AA4	000032E0			3829+ DC A(T48) test address
00004AA8	00003398			3830+ DC A(T49) test address
00004AAC	00003450			3831+ DC A(T50) test address





LOC	OBJECT	CODE	ADDR1	ADDR2	STMT				
					3868	*****			
					3869	*	Register equates		
					3870	*****			
			00000000	00000001	3872	R0	EQU	0	
			00000001	00000001	3873	R1	EQU	1	
			00000002	00000001	3874	R2	EQU	2	
			00000003	00000001	3875	R3	EQU	3	
			00000004	00000001	3876	R4	EQU	4	
			00000005	00000001	3877	R5	EQU	5	
			00000006	00000001	3878	R6	EQU	6	
			00000007	00000001	3879	R7	EQU	7	
			00000008	00000001	3880	R8	EQU	8	
			00000009	00000001	3881	R9	EQU	9	
			0000000A	00000001	3882	R10	EQU	10	
			0000000B	00000001	3883	R11	EQU	11	
			0000000C	00000001	3884	R12	EQU	12	
			0000000D	00000001	3885	R13	EQU	13	
			0000000E	00000001	3886	R14	EQU	14	
			0000000F	00000001	3887	R15	EQU	15	
					3889	*****			
					3890	*	Register equates		
					3891	*****			
			00000000	00000001	3893	V0	EQU	0	
			00000001	00000001	3894	V1	EQU	1	
			00000002	00000001	3895	V2	EQU	2	
			00000003	00000001	3896	V3	EQU	3	
			00000004	00000001	3897	V4	EQU	4	
			00000005	00000001	3898	V5	EQU	5	
			00000006	00000001	3899	V6	EQU	6	
			00000007	00000001	3900	V7	EQU	7	
			00000008	00000001	3901	V8	EQU	8	
			00000009	00000001	3902	V9	EQU	9	
			0000000A	00000001	3903	V10	EQU	10	
			0000000B	00000001	3904	V11	EQU	11	
			0000000C	00000001	3905	V12	EQU	12	
			0000000D	00000001	3906	V13	EQU	13	
			0000000E	00000001	3907	V14	EQU	14	
			0000000F	00000001	3908	V15	EQU	15	
			00000010	00000001	3909	V16	EQU	16	
			00000011	00000001	3910	V17	EQU	17	
			00000012	00000001	3911	V18	EQU	18	
			00000013	00000001	3912	V19	EQU	19	
			00000014	00000001	3913	V20	EQU	20	
			00000015	00000001	3914	V21	EQU	21	







SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
R0	U	00000000	1	3872	117	167	170	190	192	193	194	199	218	219	281	285	286
					319	327	328	353	355	371	374	376	378	380	395	691	733
					772	811	850	889	928	967	1006	1045	1084	1123	1162	1201	1240
					1279	1318	1364	1406	1445	1484	1523	1562	1601	1640	1679	1718	1757
					1796	1835	1874	1920	1962	2001	2040	2079	2118	2158	2197	2236	2275
					2314	2353	2393	2432	2471	2510	2549	2588	2628	2667	2706	2745	2784
					2823	2863	2902	2941	2980	3019	3058	3097	3136	3175	3214	3253	3292
					3332	3371	3410	3449	3488	3527	3566	3605	3644	3683	3722	3761	
					200	225	226	227	230	231	246	247	252	253	254	255	282
					320	337	338	385	399	686	687	688	689	728	729	730	731
					767	768	769	770	806	807	808	809	845	846	847	848	884
					885	886	887	923	924	925	926	962	963	964	965	1001	1002
					1003	1004	1040	1041	1042	1043	1079	1080	1081	1082	1118	1119	1120
					1121	1157	1158	1159	1160	1196	1197	1198	1199	1235	1236	1237	1238
					1274	1275	1276	1277	1313	1314	1315	1316	1359	1360	1361	1362	1401
					1402	1403	1404	1440	1441	1442	1443	1479	1480	1481	1482	1518	1519
					1520	1521	1557	1558	1559	1560	1596	1597	1598	1599	1635	1636	1637
					1638	1674	1675	1676	1677	1713	1714	1715	1716	1752	1753	1754	1755
					1791	1792	1793	1794	1830	1831	1832	1833	1869	1870	1871	1872	1915
					1916	1917	1918	1957	1958	1959	1960	1996	1997	1998	1999	2035	2036
					2037	2038	2074	2075	2076	2077	2113	2114	2115	2116	2153	2154	2155
					2156	2192	2193	2194	2195	2231	2232	2233	2234	2270	2271	2272	2273
					2309	2310	2311	2312	2348	2349	2350	2351	2388	2389	2390	2391	2427
					2428	2429	2430	2466	2467	2468	2469	2505	2506	2507	2508	2544	2545
					2546	2547	2583	2584	2585	2586	2623	2624	2625	2626	2662	2663	2664
					2665	2701	2702	2703	2704	2740	2741	2742	2743	2779	2780	2781	2782
					2818	2819	2820	2821	2858	2859	2860	2861	2897	2898	2899	2900	2936
					2937	2938	2939	2975	2976	2977	2978	3014	3015	3016	3017	3053	3054
					3055	3056	3092	3093	3094	3095	3131	3132	3133	3134	3170	3171	3172
					3173	3209	3210	3211	3212	3248	3249	3250	3251	3287	3288	3289	3290
					3327	3328	3329	3330	3366	3367	3368	3369	3405	3406	3407	3408	3444
					3445	3446	3447	3483	3484	3485	3486	3522	3523	3524	3525	3561	3562
					3563	3564	3600	3601	3602	3603	3639	3640	3641	3642	3678	3679	3680
					3681	3717	3718	3719	3720	3756	3757	3758	3759				
R10	U	0000000A	1	3882	155	164	165										
R11	U	0000000B	1	3883	222	223	694	736	775	814	853	892	931	970	1009	1048	1087
					1126	1165	1204	1243	1282	1321	1367	1409	1448	1487	1526	1565	1604
					1643	1682	1721	1760	1799	1838	1877	1923	1965	2004	2043	2082	2121
					2161	2200	2239	2278	2317	2356	2396	2435	2474	2513	2552	2591	2631
					2670	2709	2748	2787	2826	2866	2905	2944	2983	3022	3061	3100	3139
					3178	3217	3256	3295	3335	3374	3413	3452	3491	3530	3569	3608	3647
					3686	3725	3764										
R12	U	0000000C	1	3884	209	212	234	330									
R13	U	0000000D	1	3885													
R14	U	0000000E	1	3886													
R15	U	0000000F	1	3887	283	321	348	358	359								
R2	U	00000002	1	3874	201	259	260	267	268	269	274	275	276	297	298	305	306
					307	312	313	314	353	354	355	372	374	380	381	382	384
					390	395	396	691	692	733	734	772	773	811	812	850	851
					889	890	928	929	967	968	1006	1007	1045	1046	1084	1085	1123
					1124	1162	1163	1201	1202	1240	1241	1279	1280	1318	1319	1364	1365
					1406	1407	1445	1446	1484	1485	1523	1524	1562	1563	1601	1602	1640
					1641	1679	1680	1718	1719	1757	1758	1796	1797	1835	1836	1874	1875
					1920	1921	1962	1963	2001	2002	2040	2041	2079	2080	2118	2119	2158
					2159	2197	2198	2236	2237	2275	2276	2314	2315	2353	2354	2393	2394
					2432	2433	2471	2472	2510	2511	2549	2550	2588	2589	2628	2629	2667



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
RE39	F	00002CF0	4	2201	2182	2183	2184	2186	
RE4	F	000013C8	4	815	796	797	798	800	
RE40	F	00002DA8	4	2240	2221	2222	2223	2225	
RE41	F	00002E60	4	2279	2260	2261	2262	2264	
RE42	F	00002F18	4	2318	2299	2300	2301	2303	
RE43	F	00002FD0	4	2357	2338	2339	2340	2342	
RE44	F	00003088	4	2397	2378	2379	2380	2382	
RE45	F	00003140	4	2436	2417	2418	2419	2421	
RE46	F	000031F8	4	2475	2456	2457	2458	2460	
RE47	F	000032B0	4	2514	2495	2496	2497	2499	
RE48	F	00003368	4	2553	2534	2535	2536	2538	
RE49	F	00003420	4	2592	2573	2574	2575	2577	
RE5	F	00001480	4	854	835	836	837	839	
RE50	F	000034D8	4	2632	2613	2614	2615	2617	
RE51	F	00003590	4	2671	2652	2653	2654	2656	
RE52	F	00003648	4	2710	2691	2692	2693	2695	
RE53	F	00003700	4	2749	2730	2731	2732	2734	
RE54	F	000037B8	4	2788	2769	2770	2771	2773	
RE55	F	00003870	4	2827	2808	2809	2810	2812	
RE56	F	00003928	4	2867	2848	2849	2850	2852	
RE57	F	000039E0	4	2906	2887	2888	2889	2891	
RE58	F	00003A98	4	2945	2926	2927	2928	2930	
RE59	F	00003B50	4	2984	2965	2966	2967	2969	
RE6	F	00001538	4	893	874	875	876	878	
RE60	F	00003C08	4	3023	3004	3005	3006	3008	
RE61	F	00003CC0	4	3062	3043	3044	3045	3047	
RE62	F	00003D78	4	3101	3082	3083	3084	3086	
RE63	F	00003E30	4	3140	3121	3122	3123	3125	
RE64	F	00003EE8	4	3179	3160	3161	3162	3164	
RE65	F	00003FA0	4	3218	3199	3200	3201	3203	
RE66	F	00004058	4	3257	3238	3239	3240	3242	
RE67	F	00004110	4	3296	3277	3278	3279	3281	
RE68	F	000041C8	4	3336	3317	3318	3319	3321	
RE69	F	00004280	4	3375	3356	3357	3358	3360	
RE7	F	000015F0	4	932	913	914	915	917	
RE70	F	00004338	4	3414	3395	3396	3397	3399	
RE71	F	000043F0	4	3453	3434	3435	3436	3438	
RE72	F	000044A8	4	3492	3473	3474	3475	3477	
RE73	F	00004560	4	3531	3512	3513	3514	3516	
RE74	F	00004618	4	3570	3551	3552	3553	3555	
RE75	F	000046D0	4	3609	3590	3591	3592	3594	
RE76	F	00004788	4	3648	3629	3630	3631	3633	
RE77	F	00004840	4	3687	3668	3669	3670	3672	
RE78	F	000048F8	4	3726	3707	3708	3709	3711	
RE79	F	000049B0	4	3765	3746	3747	3748	3750	
RE8	F	000016A8	4	971	952	953	954	956	
RE9	F	00001760	4	1010	991	992	993	995	
REA1	A	00001148	4	680					
REA10	A	000017C0	4	1034					
REA11	A	00001878	4	1073					
REA12	A	00001930	4	1112					
REA13	A	000019E8	4	1151					
REA14	A	00001AA0	4	1190					
REA15	A	00001B58	4	1229					
REA16	A	00001C10	4	1268					
REA17	A	00001CC8	4	1307					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA18	A	00001D80	4	1353	
REA19	A	00001E38	4	1395	
REA2	A	00001200	4	722	
REA20	A	00001EF0	4	1434	
REA21	A	00001FA8	4	1473	
REA22	A	00002060	4	1512	
REA23	A	00002118	4	1551	
REA24	A	000021D0	4	1590	
REA25	A	00002288	4	1629	
REA26	A	00002340	4	1668	
REA27	A	000023F8	4	1707	
REA28	A	000024B0	4	1746	
REA29	A	00002568	4	1785	
REA3	A	000012B8	4	761	
REA30	A	00002620	4	1824	
REA31	A	000026D8	4	1863	
REA32	A	00002790	4	1909	
REA33	A	00002848	4	1951	
REA34	A	00002900	4	1990	
REA35	A	000029B8	4	2029	
REA36	A	00002A70	4	2068	
REA37	A	00002B28	4	2107	
REA38	A	00002BE0	4	2147	
REA39	A	00002C98	4	2186	
REA4	A	00001370	4	800	
REA40	A	00002D50	4	2225	
REA41	A	00002E08	4	2264	
REA42	A	00002EC0	4	2303	
REA43	A	00002F78	4	2342	
REA44	A	00003030	4	2382	
REA45	A	000030E8	4	2421	
REA46	A	000031A0	4	2460	
REA47	A	00003258	4	2499	
REA48	A	00003310	4	2538	
REA49	A	000033C8	4	2577	
REA5	A	00001428	4	839	
REA50	A	00003480	4	2617	
REA51	A	00003538	4	2656	
REA52	A	000035F0	4	2695	
REA53	A	000036A8	4	2734	
REA54	A	00003760	4	2773	
REA55	A	00003818	4	2812	
REA56	A	000038D0	4	2852	
REA57	A	00003988	4	2891	
REA58	A	00003A40	4	2930	
REA59	A	00003AF8	4	2969	
REA6	A	000014E0	4	878	
REA60	A	00003BB0	4	3008	
REA61	A	00003C68	4	3047	
REA62	A	00003D20	4	3086	
REA63	A	00003DD8	4	3125	
REA64	A	00003E90	4	3164	
REA65	A	00003F48	4	3203	
REA66	A	00004000	4	3242	
REA67	A	000040B8	4	3281	
REA68	A	00004170	4	3321	



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA69	A	00004228	4	3360		
REA7	A	00001598	4	917		
REA70	A	000042E0	4	3399		
REA71	A	00004398	4	3438		
REA72	A	00004450	4	3477		
REA73	A	00004508	4	3516		
REA74	A	000045C0	4	3555		
REA75	A	00004678	4	3594		
REA76	A	00004730	4	3633		
REA77	A	000047E8	4	3672		
REA78	A	000048A0	4	3711		
REA79	A	00004958	4	3750		
REA8	A	00001650	4	956		
REA9	A	00001708	4	995		
READDR	A	00000030	4	531	230	
REG2LOW	U	000000DD	1	441		
REG2PATT	U	AABBCCDD	1	440		
RELEN	A	0000002C	4	530		
RPTDWSAV	D	00000460	8	364	353	355
RPTERROR	I	00000436	4	348	283	321
RPTSAVE	F	00000454	4	361	348	358
RPTSVR5	F	00000458	4	362	349	357
SKL0001	U	0000004E	1	183	199	
SKT0001	C	0000022A	20	180	183	200
SVOLDPSW	U	00000140	0	119		
T1	A	00001118	4	666	3782	
T10	A	00001790	4	1020	3791	
T11	A	00001848	4	1059	3792	
T12	A	00001900	4	1098	3793	
T13	A	000019B8	4	1137	3794	
T14	A	00001A70	4	1176	3795	
T15	A	00001B28	4	1215	3796	
T16	A	00001BE0	4	1254	3797	
T17	A	00001C98	4	1293	3798	
T18	A	00001D50	4	1339	3799	
T19	A	00001E08	4	1381	3800	
T2	A	000011D0	4	708	3783	
T20	A	00001EC0	4	1420	3801	
T21	A	00001F78	4	1459	3802	
T22	A	00002030	4	1498	3803	
T23	A	000020E8	4	1537	3804	
T24	A	000021A0	4	1576	3805	
T25	A	00002258	4	1615	3806	
T26	A	00002310	4	1654	3807	
T27	A	000023C8	4	1693	3808	
T28	A	00002480	4	1732	3809	
T29	A	00002538	4	1771	3810	
T3	A	00001288	4	747	3784	
T30	A	000025F0	4	1810	3811	
T31	A	000026A8	4	1849	3812	
T32	A	00002760	4	1895	3813	
T33	A	00002818	4	1937	3814	
T34	A	000028D0	4	1976	3815	
T35	A	00002988	4	2015	3816	
T36	A	00002A40	4	2054	3817	
T37	A	00002AF8	4	2093	3818	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
T38	A	00002BB0	4	2133	3819		
T39	A	00002C68	4	2172	3820		
T4	A	00001340	4	786	3785		
T40	A	00002D20	4	2211	3821		
T41	A	00002DD8	4	2250	3822		
T42	A	00002E90	4	2289	3823		
T43	A	00002F48	4	2328	3824		
T44	A	00003000	4	2368	3825		
T45	A	000030B8	4	2407	3826		
T46	A	00003170	4	2446	3827		
T47	A	00003228	4	2485	3828		
T48	A	000032E0	4	2524	3829		
T49	A	00003398	4	2563	3830		
T5	A	000013F8	4	825	3786		
T50	A	00003450	4	2603	3831		
T51	A	00003508	4	2642	3832		
T52	A	000035C0	4	2681	3833		
T53	A	00003678	4	2720	3834		
T54	A	00003730	4	2759	3835		
T55	A	000037E8	4	2798	3836		
T56	A	000038A0	4	2838	3837		
T57	A	00003958	4	2877	3838		
T58	A	00003A10	4	2916	3839		
T59	A	00003AC8	4	2955	3840		
T6	A	000014B0	4	864	3787		
T60	A	00003B80	4	2994	3841		
T61	A	00003C38	4	3033	3842		
T62	A	00003CF0	4	3072	3843		
T63	A	00003DA8	4	3111	3844		
T64	A	00003E60	4	3150	3845		
T65	A	00003F18	4	3189	3846		
T66	A	00003FD0	4	3228	3847		
T67	A	00004088	4	3267	3848		
T68	A	00004140	4	3307	3849		
T69	A	000041F8	4	3346	3850		
T7	A	00001568	4	903	3788		
T70	A	000042B0	4	3385	3851		
T71	A	00004368	4	3424	3852		
T72	A	00004420	4	3463	3853		
T73	A	000044D8	4	3502	3854		
T74	A	00004590	4	3541	3855		
T75	A	00004648	4	3580	3856		
T76	A	00004700	4	3619	3857		
T77	A	000047B8	4	3658	3858		
T78	A	00004870	4	3697	3859		
T79	A	00004928	4	3736	3860		
T8	A	00001620	4	942	3789		
T9	A	000016D8	4	981	3790		
TESTCC	I	00000318	4	237	227		
TESTING	F	00001004	4	452	219		
TESTREST	U	00000300	1	229	248	288	
TNUM	H	00000004	2	514	218	259	297
TSUB	A	00000000	4	513	222		
TTABLE	F	000049E8	4	3781			
V0	U	00000000	1	3893			
V1	U	00000001	1	3894			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10	U	0000000A	1	3903	
V11	U	0000000B	1	3904	
V12	U	0000000C	1	3905	
V13	U	0000000D	1	3906	
V14	U	0000000E	1	3907	
V15	U	0000000F	1	3908	
V16	U	00000010	1	3909	
V17	U	00000011	1	3910	
V18	U	00000012	1	3911	
V19	U	00000013	1	3912	
V1ADDR	A	00000020	4	527	
V1FUDGE	X	000010F8	16	505	221
V101	X	00001158	16	682	693
V1010	X	000017D0	16	1036	1047
V1011	X	00001888	16	1075	1086
V1012	X	00001940	16	1114	1125
V1013	X	000019F8	16	1153	1164
V1014	X	00001AB0	16	1192	1203
V1015	X	00001B68	16	1231	1242
V1016	X	00001C20	16	1270	1281
V1017	X	00001CD8	16	1309	1320
V1018	X	00001D90	16	1355	1366
V1019	X	00001E48	16	1397	1408
V102	X	00001210	16	724	735
V1020	X	00001F00	16	1436	1447
V1021	X	00001FB8	16	1475	1486
V1022	X	00002070	16	1514	1525
V1023	X	00002128	16	1553	1564
V1024	X	000021E0	16	1592	1603
V1025	X	00002298	16	1631	1642
V1026	X	00002350	16	1670	1681
V1027	X	00002408	16	1709	1720
V1028	X	000024C0	16	1748	1759
V1029	X	00002578	16	1787	1798
V103	X	000012C8	16	763	774
V1030	X	00002630	16	1826	1837
V1031	X	000026E8	16	1865	1876
V1032	X	000027A0	16	1911	1922
V1033	X	00002858	16	1953	1964
V1034	X	00002910	16	1992	2003
V1035	X	000029C8	16	2031	2042
V1036	X	00002A80	16	2070	2081
V1037	X	00002B38	16	2109	2120
V1038	X	00002BF0	16	2149	2160
V1039	X	00002CA8	16	2188	2199
V104	X	00001380	16	802	813
V1040	X	00002D60	16	2227	2238
V1041	X	00002E18	16	2266	2277
V1042	X	00002ED0	16	2305	2316
V1043	X	00002F88	16	2344	2355
V1044	X	00003040	16	2384	2395
V1045	X	000030F8	16	2423	2434
V1046	X	000031B0	16	2462	2473
V1047	X	00003268	16	2501	2512
V1048	X	00003320	16	2540	2551
V1049	X	000033D8	16	2579	2590

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
V105	X	00001438	16	841	852													
V1050	X	00003490	16	2619	2630													
V1051	X	00003548	16	2658	2669													
V1052	X	00003600	16	2697	2708													
V1053	X	000036B8	16	2736	2747													
V1054	X	00003770	16	2775	2786													
V1055	X	00003828	16	2814	2825													
V1056	X	000038E0	16	2854	2865													
V1057	X	00003998	16	2893	2904													
V1058	X	00003A50	16	2932	2943													
V1059	X	00003B08	16	2971	2982													
V106	X	000014F0	16	880	891													
V1060	X	00003BC0	16	3010	3021													
V1061	X	00003C78	16	3049	3060													
V1062	X	00003D30	16	3088	3099													
V1063	X	00003DE8	16	3127	3138													
V1064	X	00003EA0	16	3166	3177													
V1065	X	00003F58	16	3205	3216													
V1066	X	00004010	16	3244	3255													
V1067	X	000040C8	16	3283	3294													
V1068	X	00004180	16	3323	3334													
V1069	X	00004238	16	3362	3373													
V107	X	000015A8	16	919	930													
V1070	X	000042F0	16	3401	3412													
V1071	X	000043A8	16	3440	3451													
V1072	X	00004460	16	3479	3490													
V1073	X	00004518	16	3518	3529													
V1074	X	000045D0	16	3557	3568													
V1075	X	00004688	16	3596	3607													
V1076	X	00004740	16	3635	3646													
V1077	X	000047F8	16	3674	3685													
V1078	X	000048B0	16	3713	3724													
V1079	X	00004968	16	3752	3763													
V108	X	00001660	16	958	969													
V109	X	00001718	16	997	1008													
V10UTPUT	X	00000040	16	533	231													
V2	U	00000002	1	3895														
V20	U	00000014	1	3913														
V21	U	00000015	1	3914	690	693	732	735	771	774	810	813	849	852	888	891	927	
					930	966	969	1005	1008	1044	1047	1083	1086	1122	1125	1161	1164	
					1200	1203	1239	1242	1278	1281	1317	1320	1363	1366	1405	1408	1444	
					1447	1483	1486	1522	1525	1561	1564	1600	1603	1639	1642	1678	1681	
					1717	1720	1756	1759	1795	1798	1834	1837	1873	1876	1919	1922	1961	
					1964	2000	2003	2039	2042	2078	2081	2117	2120	2157	2160	2196	2199	
					2235	2238	2274	2277	2313	2316	2352	2355	2392	2395	2431	2434	2470	
					2473	2509	2512	2548	2551	2587	2590	2627	2630	2666	2669	2705	2708	
					2744	2747	2783	2786	2822	2825	2862	2865	2901	2904	2940	2943	2979	
					2982	3018	3021	3057	3060	3096	3099	3135	3138	3174	3177	3213	3216	
					3252	3255	3291	3294	3331	3334	3370	3373	3409	3412	3448	3451	3487	
					3490	3526	3529	3565	3568	3604	3607	3643	3646	3682	3685	3721	3724	
					3760	3763												
V22	U	00000016	1	3915	221	687	690	729	732	768	771	807	810	846	849	885	888	
					924	927	963	966	1002	1005	1041	1044	1080	1083	1119	1122	1158	
					1161	1197	1200	1236	1239	1275	1278	1314	1317	1360	1363	1402	1405	
					1441	1444	1480	1483	1519	1522	1558	1561	1597	1600	1636	1639	1675	
					1678	1714	1717	1753	1756	1792	1795	1831	1834	1870	1873	1916	1919	





SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X14	F	00001AC8	4	1195	1176
X15	F	00001B80	4	1234	1215
X16	F	00001C38	4	1273	1254
X17	F	00001CF0	4	1312	1293
X18	F	00001DA8	4	1358	1339
X19	F	00001E60	4	1400	1381
X2	F	00001228	4	727	708
X20	F	00001F18	4	1439	1420
X21	F	00001FD0	4	1478	1459
X22	F	00002088	4	1517	1498
X23	F	00002140	4	1556	1537
X24	F	000021F8	4	1595	1576
X25	F	000022B0	4	1634	1615
X26	F	00002368	4	1673	1654
X27	F	00002420	4	1712	1693
X28	F	000024D8	4	1751	1732
X29	F	00002590	4	1790	1771
X3	F	000012E0	4	766	747
X30	F	00002648	4	1829	1810
X31	F	00002700	4	1868	1849
X32	F	000027B8	4	1914	1895
X33	F	00002870	4	1956	1937
X34	F	00002928	4	1995	1976
X35	F	000029E0	4	2034	2015
X36	F	00002A98	4	2073	2054
X37	F	00002B50	4	2112	2093
X38	F	00002C08	4	2152	2133
X39	F	00002CC0	4	2191	2172
X4	F	00001398	4	805	786
X40	F	00002D78	4	2230	2211
X41	F	00002E30	4	2269	2250
X42	F	00002EE8	4	2308	2289
X43	F	00002FA0	4	2347	2328
X44	F	00003058	4	2387	2368
X45	F	00003110	4	2426	2407
X46	F	000031C8	4	2465	2446
X47	F	00003280	4	2504	2485
X48	F	00003338	4	2543	2524
X49	F	000033F0	4	2582	2563
X5	F	00001450	4	844	825
X50	F	000034A8	4	2622	2603
X51	F	00003560	4	2661	2642
X52	F	00003618	4	2700	2681
X53	F	000036D0	4	2739	2720
X54	F	00003788	4	2778	2759
X55	F	00003840	4	2817	2798
X56	F	000038F8	4	2857	2838
X57	F	000039B0	4	2896	2877
X58	F	00003A68	4	2935	2916
X59	F	00003B20	4	2974	2955
X6	F	00001508	4	883	864
X60	F	00003BD8	4	3013	2994
X61	F	00003C90	4	3052	3033
X62	F	00003D48	4	3091	3072
X63	F	00003E00	4	3130	3111
X64	F	00003EB8	4	3169	3150

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
X65	F	00003F70	4	3208	3189					
X66	F	00004028	4	3247	3228					
X67	F	000040E0	4	3286	3267					
X68	F	00004198	4	3326	3307					
X69	F	00004250	4	3365	3346					
X7	F	000015C0	4	922	903					
X70	F	00004308	4	3404	3385					
X71	F	000043C0	4	3443	3424					
X72	F	00004478	4	3482	3463					
X73	F	00004530	4	3521	3502					
X74	F	000045E8	4	3560	3541					
X75	F	000046A0	4	3599	3580					
X76	F	00004758	4	3638	3619					
X77	F	00004810	4	3677	3658					
X78	F	000048C8	4	3716	3697					
X79	F	00004980	4	3755	3736					
X8	F	00001678	4	961	942					
X9	F	00001730	4	1000	981					
XC0001	U	000002D0	1	203	195					
ZVE7TST	J	00000000	19252	116	119	121	125	129	450	117
=A(E7TESTS)	A	0000056C	4	427	209					
=AL2(L' MSGMSG)	R	0000057A	2	431	376					
=D' 1'	D	00000560	8	425	247					
=F' 1'	F	00000574	4	429	285	327				
=F' 64'	F	00000568	4	426	194					
=H' 0'	H	00000578	2	430	371					
=XL4' 3'	X	00000570	4	428	254					





DESC	SYMBOL	SIZE	POS	ADDR
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**Entry: 0**

<b>Image</b>	<b>IMAGE</b>	<b>19252</b>	<b>0000- 4B33</b>	<b>0000- 4B33</b>
<b>Regi on</b>		<b>19252</b>	<b>0000- 4B33</b>	<b>0000- 4B33</b>
<b>CSECT</b>	<b>ZVE7TST</b>	<b>19252</b>	<b>0000- 4B33</b>	<b>0000- 4B33</b>

STMT	FILE NAME
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```
1 /home/tn529/sharedvfp/tests/zvector-e7-06-Find.asm
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**\*\* NO ERRORS FOUND \*\***